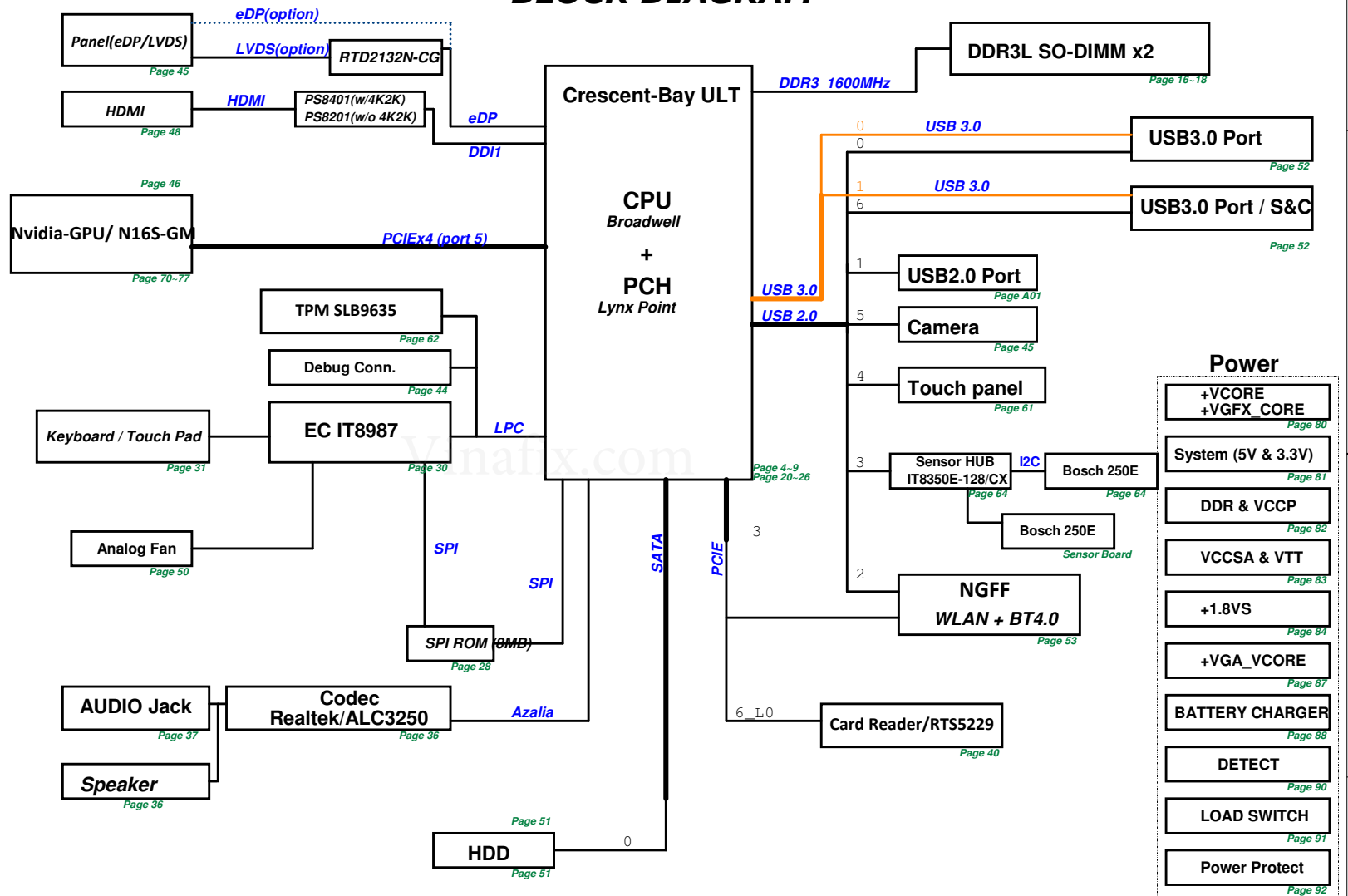


01. Block Diagram  
 02. System Setting  
 04. CPU(2)\_MISC, JTAG, DDI, EDP  
 05. CPU(3)\_DDR3L  
 06. CPU(4)\_HSW POWER  
 08. CPU(6)\_GND  
 09. CPU(7)\_RESERVED  
 16. DDR3(1)\_SO-DIMM0  
 17. DDR3(2)\_SO-DIMM1  
 18. DDR3(3)\_CA/DQ Voltage  
 20. PCH(1)\_SATA, IHD, RTC  
 21. PCH(2)\_CLK, SMB, LPC  
 22. PCH(3)\_SYS PWR  
 23. PCH(4)\_DP, PCI, CRT  
 24. PCH(5)\_PCIE, NVRAM, USB  
 25. PCH(6)\_CPU, GPIO, MISC  
 26. PCH(7)\_POWER, GND  
 28. PCH(9)\_SPI, SMB  
 30. EC\_IT8528E/FX  
 31. TP / Keyboard  
 32. RST\_Reset Circuit  
 33. LAN-RTL8111G/8106E  
 34. LAN\_RJ45  
 36. AUDIO\_ALC233  
 37. AUDIO\_Combio JACK  
 40. CB(1)\_AU6601  
 44. BUG\_Debug  
 45. LVDS\_output  
 46. DP to CRT IT6513  
 48. TV(1)\_HDMI-4K2K  
 50. THERMAL / FAN  
 51. SATA HDD/ ODD  
 52. USB JACK  
 53. MINICARD\_WLAN  
 56. LED\_Indicator  
 57. Discharge  
 58. G-sensor  
 60. DC\_DC/BAT CONN  
 62. NFC CONNECTOR  
 65. ME\_CONN, Skew Hole  
 66. PWR BRD/ IO BRD  
 70. AMD\_GPU-S3-PCIE  
 71. AMD\_GPU-S3-HDMI/DAC/LVDS  
 72. AMD\_GPU-S3-(1)MEM\_CTRL\_CHA  
 74. AMD\_GPU-S3-STRAP\_MISC  
 75. AMD\_GPU-S3-(1)POWER/GND  
 76. AMD\_GPU-S3-(2)DP POWER  
 77. AMD\_GPU-S3-MEM\_CHA  
 78. AMD\_GPU-S3-MEM\_CHB  
 79. AMD\_GPU-S3-POWER FLOW  
 80. POWER\_VCORE  
 81. POWER\_SYSTEM  
 82. POWER\_+1.05VS  
 83. POWER\_DDR & VTT  
 84. POWER\_1.8VS  
 86. POWER\_1.5VS  
 87. POWER\_VGA\_VCORE\_2PHASE  
 88. POWER\_CHARGER  
 89. POWER\_\*\*\*\*  
 90. POWER\_DETECT  
 91. POWER\_LOAD SWITCH  
 92. POWER\_PROTECT  
 93. POWER\_SIGNAL

# TRCUG with Broadwell ULT

## BLOCK DIAGRAM



Discharge Circuit

Page 57

Reset Circuit

Page 32

DC &amp; BATT. Conn.

Page 60

Skew Holes

Page 65

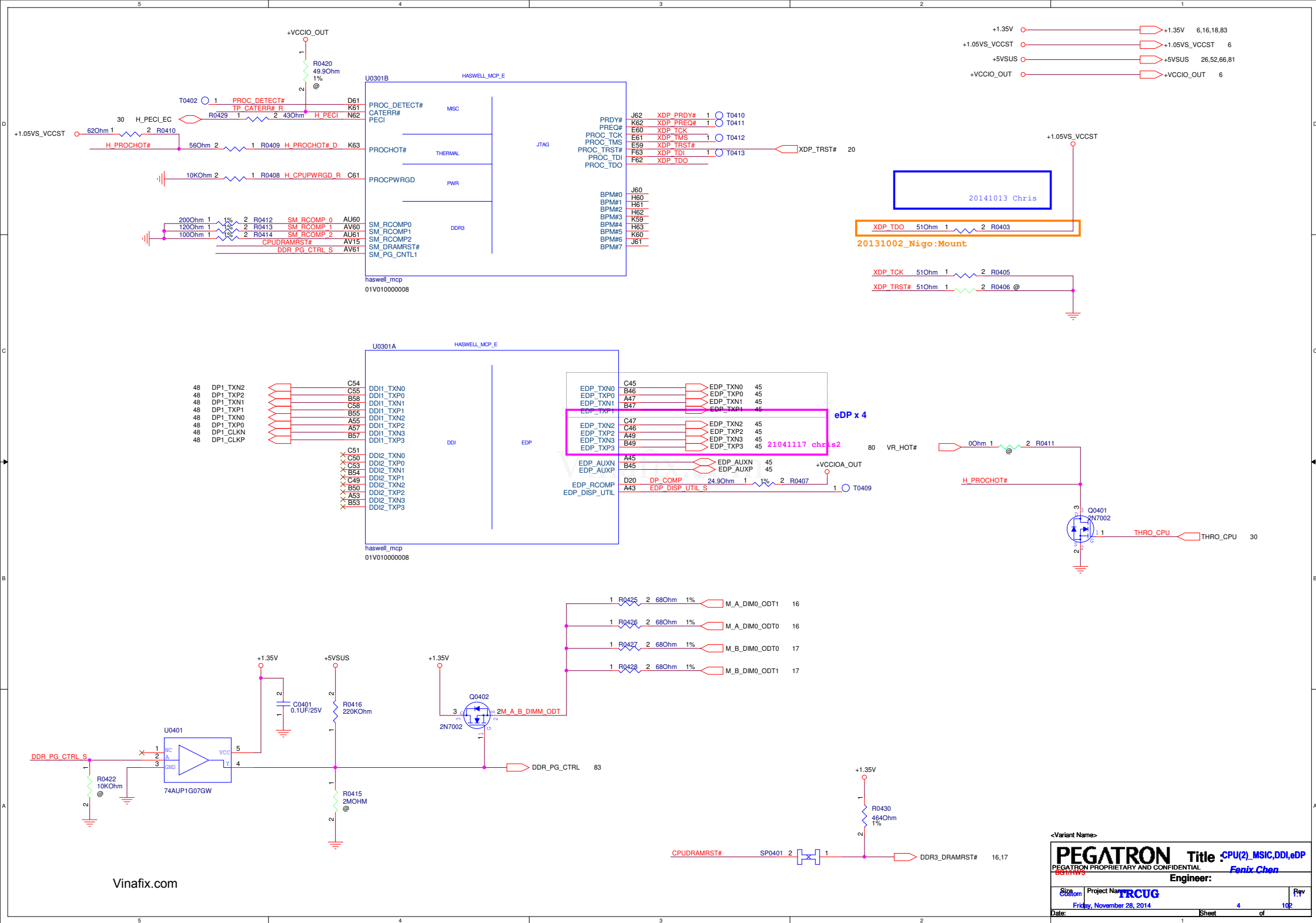
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Vinafix.com

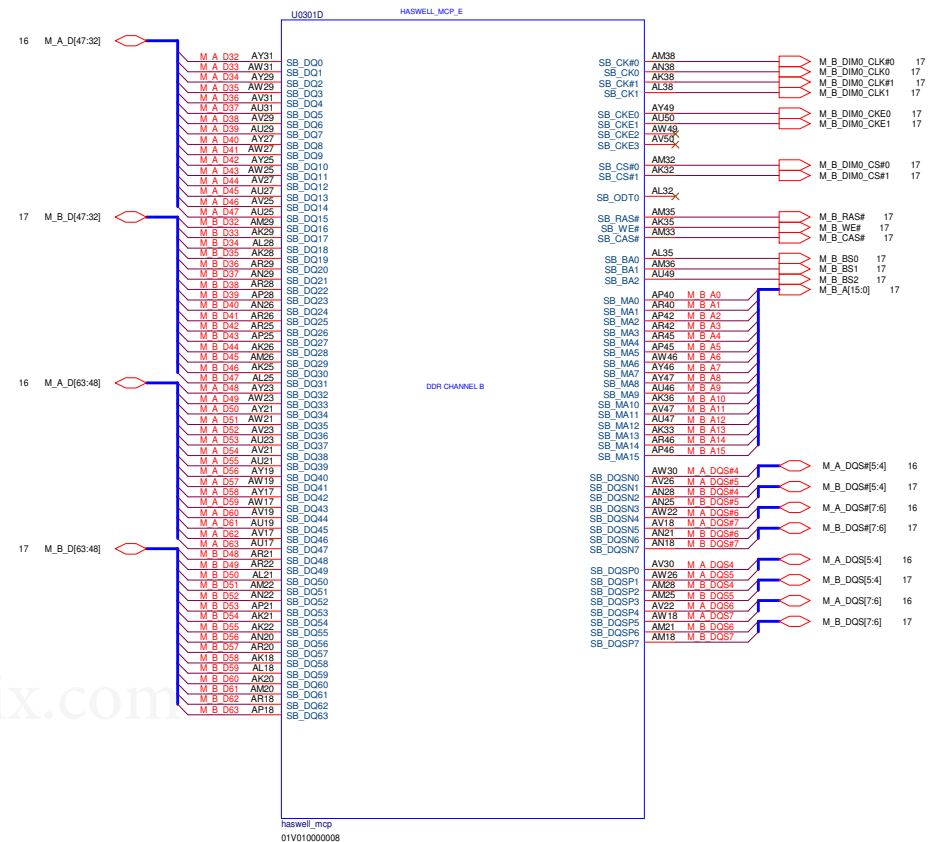
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Size	Project Name		Rev. 1
Date		Friday, November 28, 2014	1
Sheet		2	of 102

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PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:			
Size	Project Name	Rev.	
	Friday, November 28, 2014	3	102
Date	Sheet		of



## DDR interleave routing



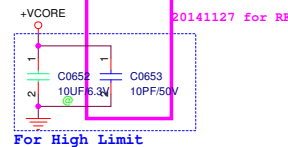
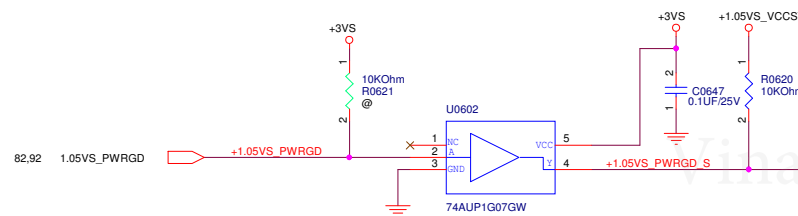
20141127 For RF  
 Checklist: 470uF\*2  
 Caps: reserfe 10uF\*6

CPU: 1.4A, DIMM: 4.4A  
 Checklist: 2.2uF\*4, 10uF\*10

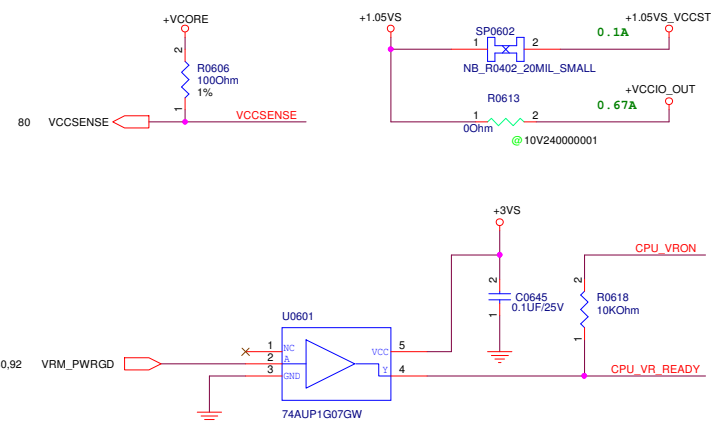
For High Limit, Change to 100uF\*2

For High Limit

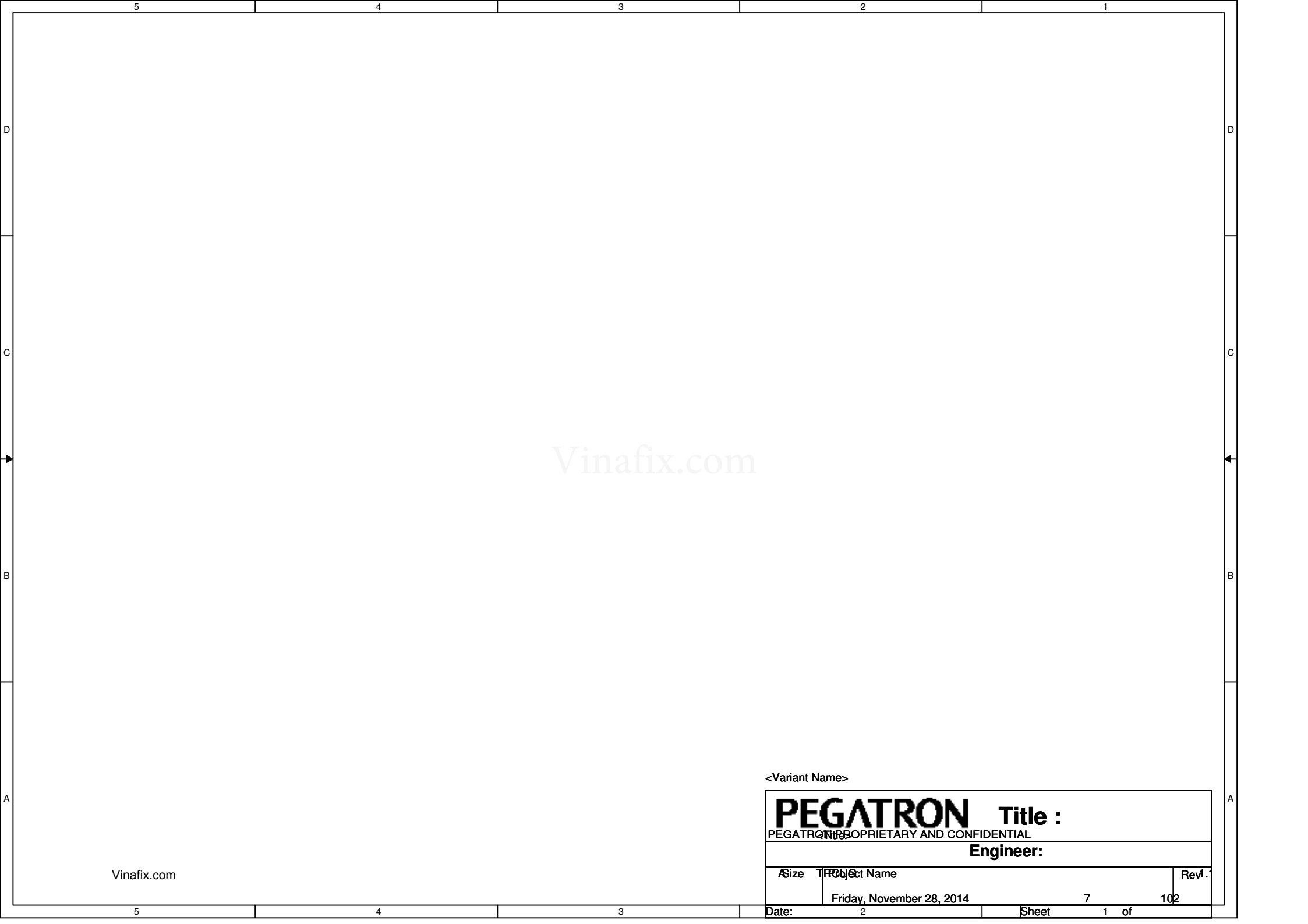
For High Limit  
 Change to 100uF\*2



**+VCORE 32A**  
**Intel Checklist: used 30pcs(7pcs un-used)**  
**Power side: 20pcs (4pcs un-used)**  
**VGST: 30pcs (14pcs un-used)**



+1.35V	4,16,18,83
+1.05VS_VCCST	4
+VCORE	80
+3VS	16,17,20,21,22,23,25,26,28,30,31,36,37,40,45,48,50,53,57,61,62,64,66,80,91,92
+1.05VS	25,26,80,82

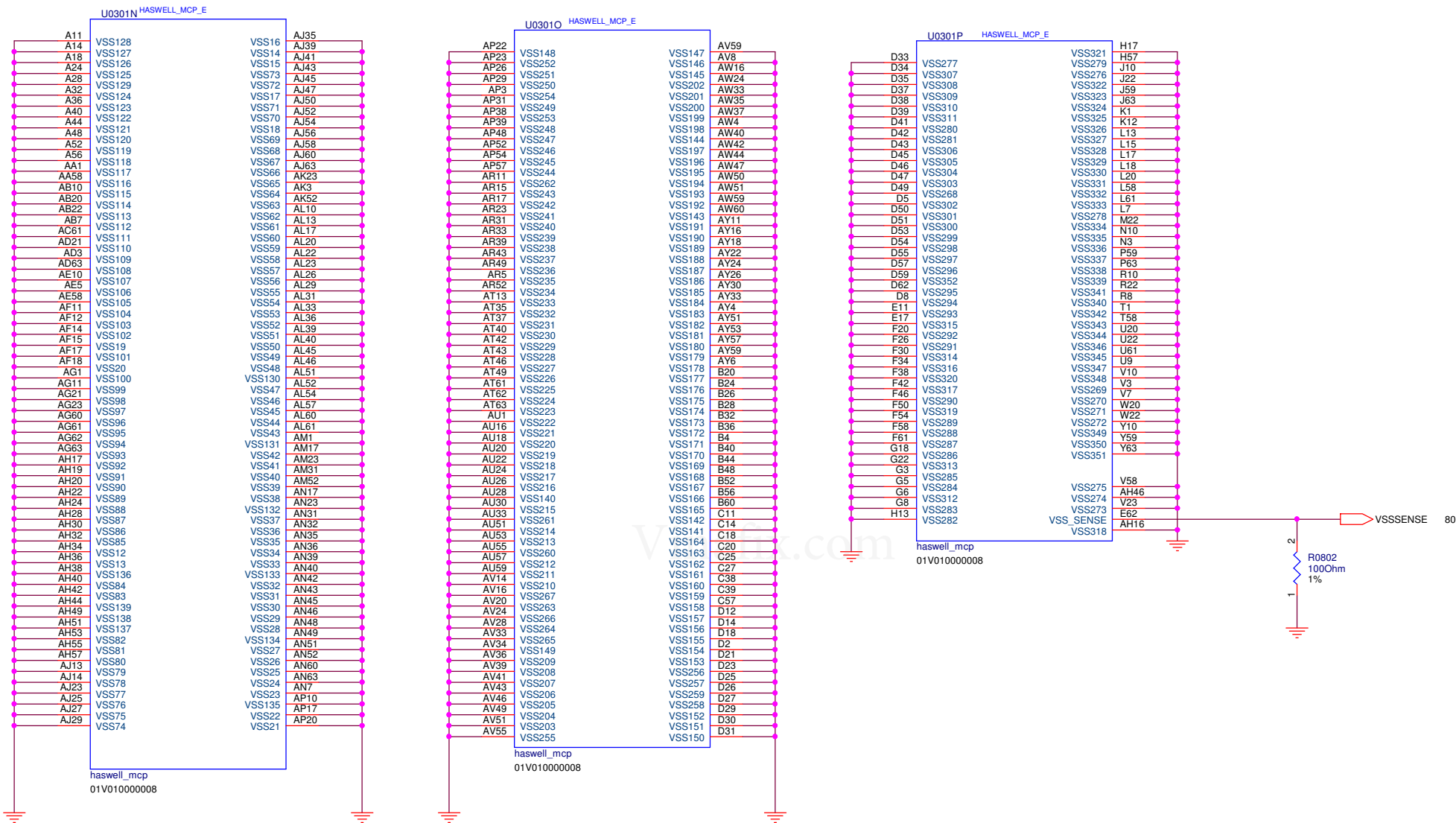


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Engineer:		
Size	Project Name	Rev.
	Friday, November 28, 2014	7 102
Date:	2	Sheet 1 of 102

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		<b>Engineer:</b>	
Size	Project Name		Rev.
	Friday, November 28, 2014	10	102
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Engineer:			
Size	Project Name	Rev.	
	Friday, November 28, 2014	11	102
Date	Sheet		of

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Size	Project Name		Rev.
	Friday, November 28, 2014	12	102
Date	Sheet		of

Vinafix.com

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PEGATRON PROPRIETARY AND CONFIDENTIAL			
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Size	Project Name		Rev.
	Friday, November 28, 2014	13	102
Date	Sheet		of

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PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:			
Size	Project Name	Rev.	
	Friday, November 28, 2014	14	102
Date	Sheet		of

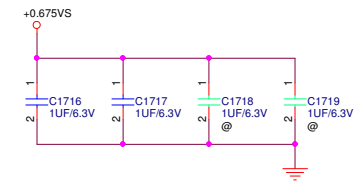
Vinafix.com

Vinafix.com

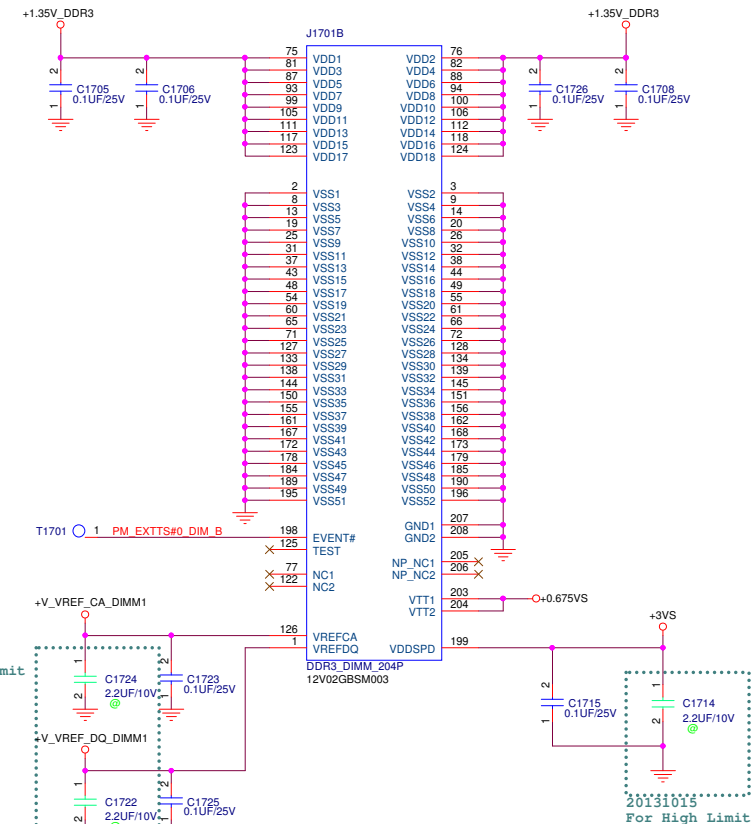
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer:</b>	
Size	Project Name		Rev.
	Friday, November 28, 2014	15	102
Date	Sheet		of



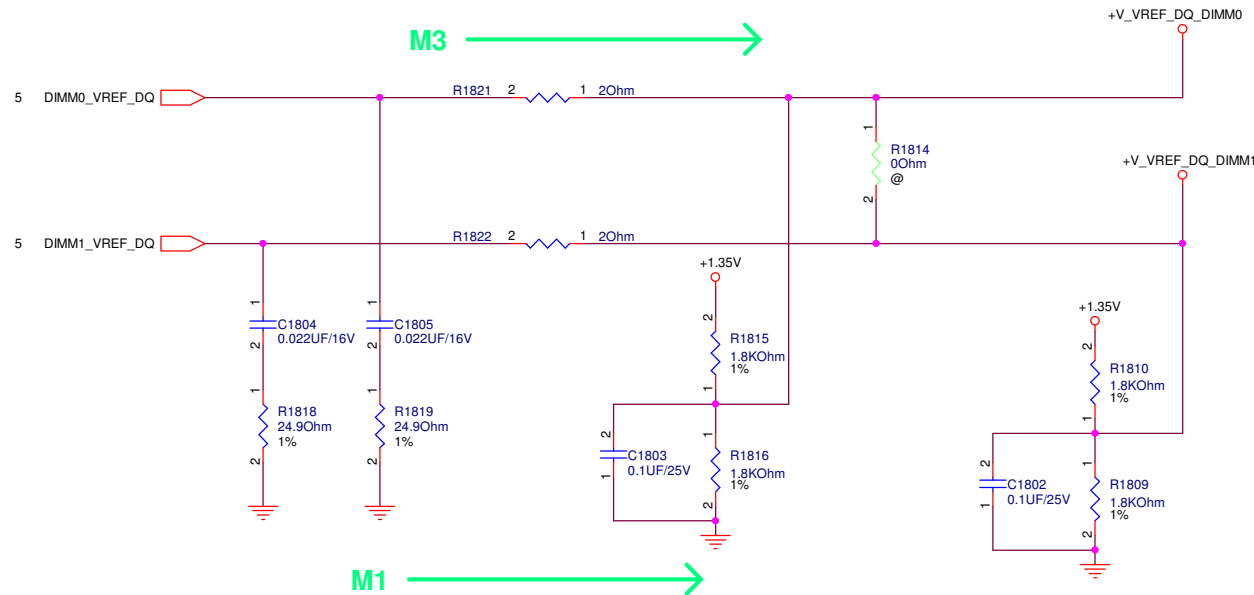




***H:4mm STD***



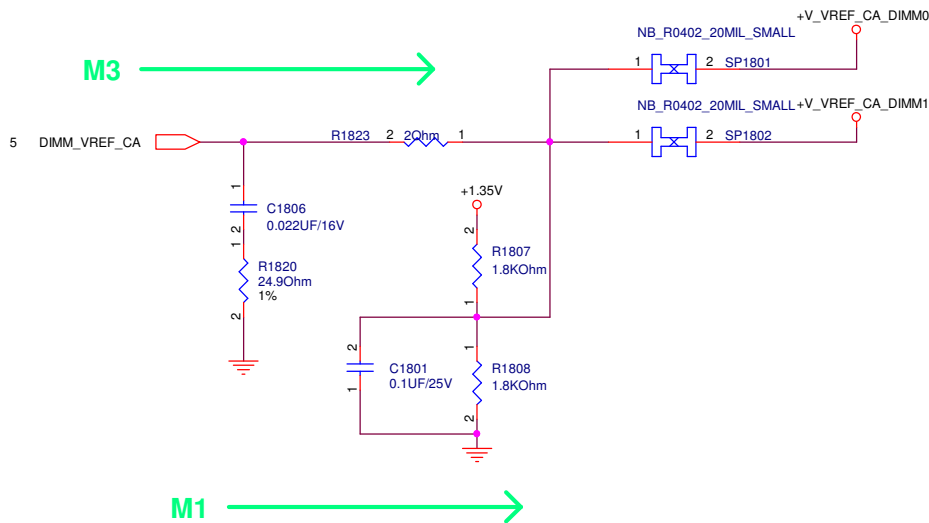
M3: CPU driven VREF path is stuffed be default.  
M1: VREF\_DQ driven by a Voltage Divider Network during Processor power-off



+V_VREF_DQ_DIMM0	→	+V_VREF_DQ_DIMM0	16
+V_VREF_DQ_DIMM1	→	+V_VREF_DQ_DIMM1	17
+1.35V	→	+1.35V	4,6,16,83
+V_VREF_CA_DIMM0	→	+V_VREF_CA_DIMM0	16
+V_VREF_CA_DIMM1	→	+V_VREF_CA_DIMM1	17

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For meet the Intel Design Guide  
Change to 2 OHM: R1821, R1822, R1823  
Change to 1.8K ohm: R1809, R1810, R1815, R1816, R1807, R1808

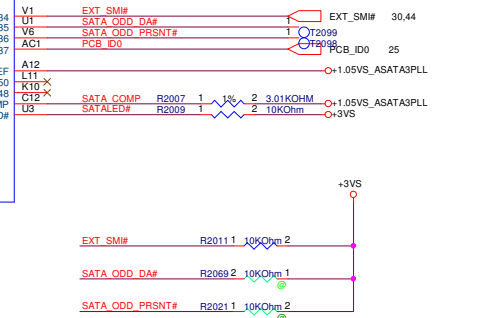
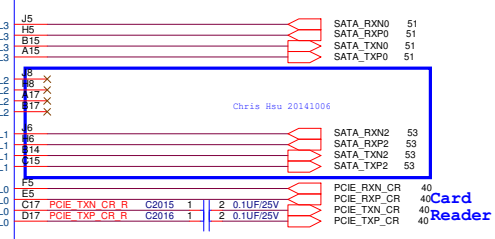
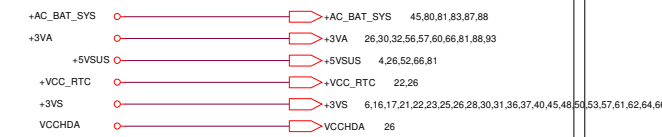


<Variant Name>		Title	
PEGATRON		DDR3(3)_CA/DQ Voltage	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BGT/HWS		Fenix Chen	
Engineer:			
Size	Project Name	Rev	
8	TRCUG		
Date: Friday, November 28, 2014		Sheet	18 of 102

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<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer:</b>	
Size	Project Name		Rev.
	Friday, November 28, 2014	19	102
Date	Sheet		of



NB\_R0402\_20MIL\_SMALL

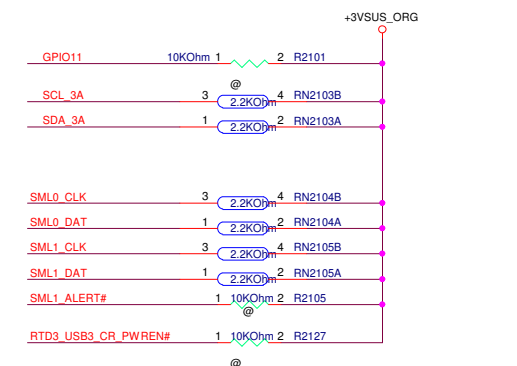
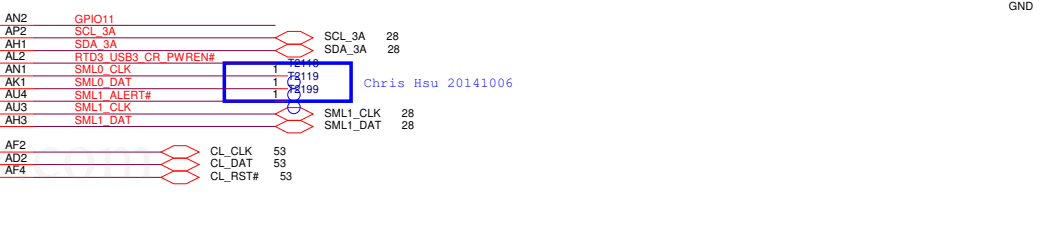
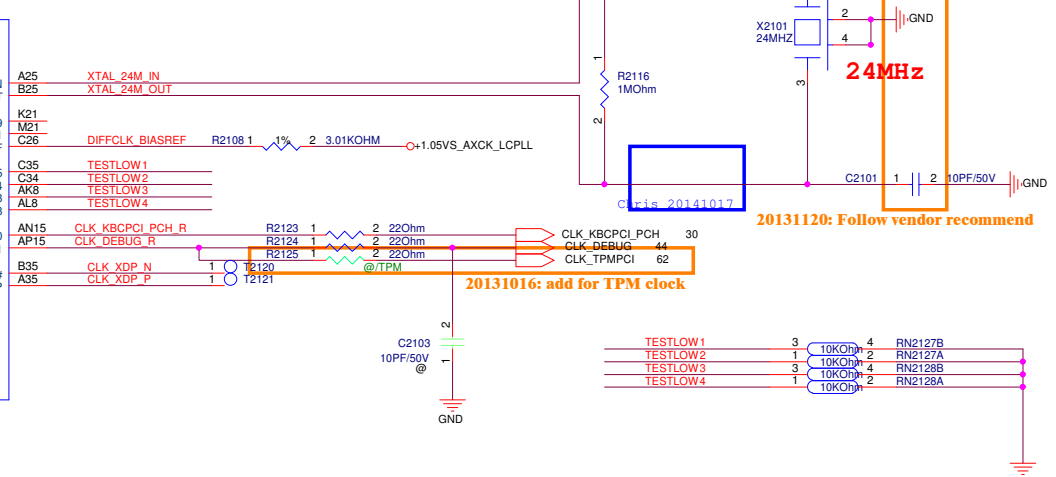
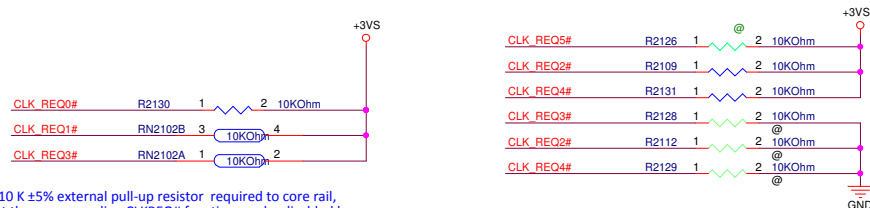
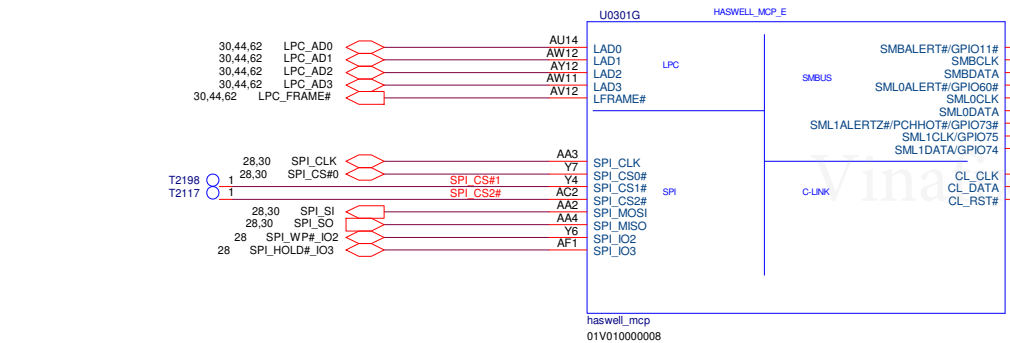
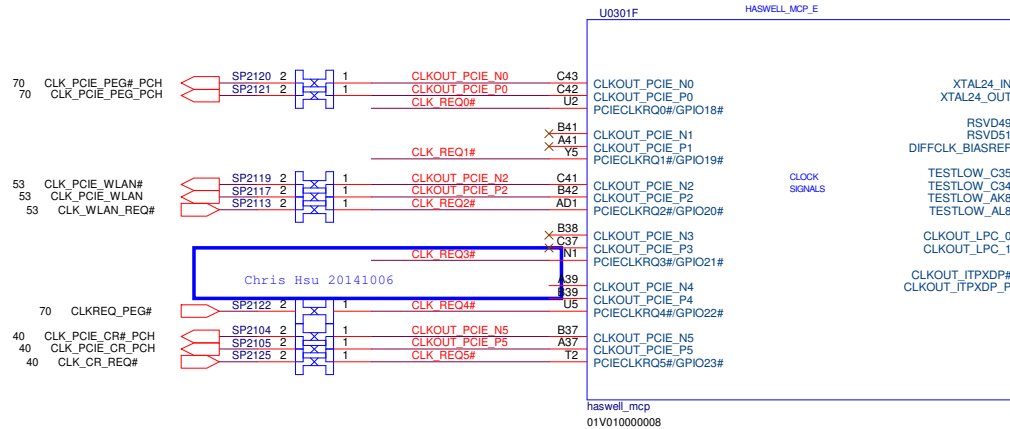
1 2 R2058 HDA SYNC R

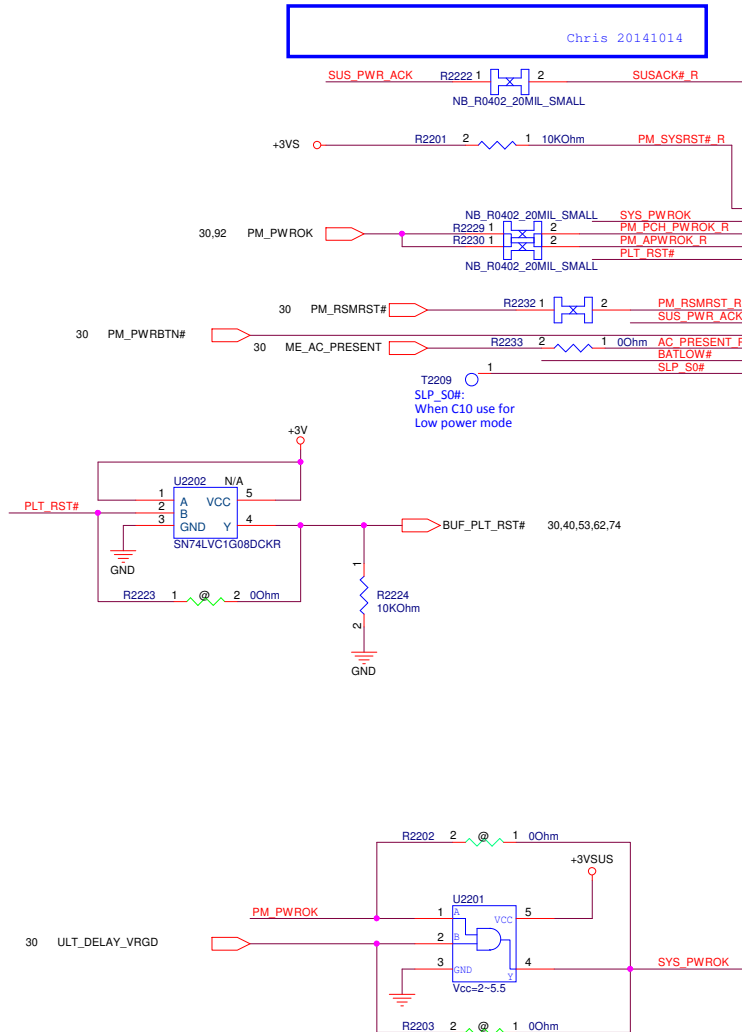
reserved Leakage

20131020: remove MOS



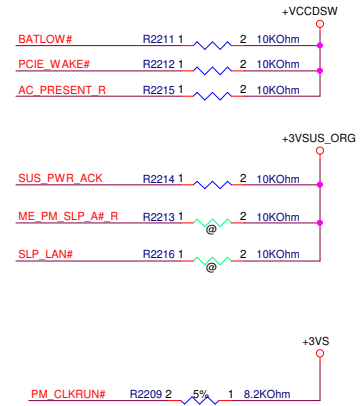
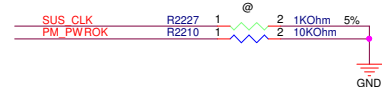
+3VS → +3VS 6,16,17,20,22,23,25,26,28,30,31,36,37,40,45,48,50,53,57,61,62,64,66,80,91,92  
+3VSUS\_ORG → +3VSUS\_ORG 22,24,25,26





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- +3VS 6,16,17,20,21,23,25,26,28,30,31,36,37,40,45,48,50,53,57,61,62,64,66,80,91,92
- +3VSUS\_ORG 21,24,25,26
- +VCCDSW 25,26
- +3V 25,31,44,64,66,91



<Variant Name>

**PEGATRON** Title PCH(3)\_FDI,DMI,SYS P

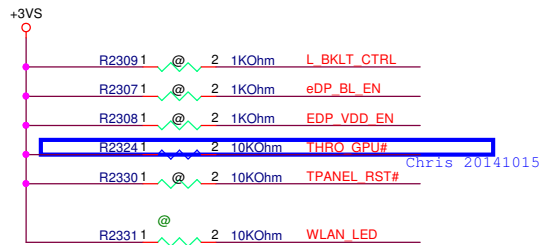
PEGATRON PROPRIETARY AND CONFIDENTIAL

Engineer: Fenix Chen

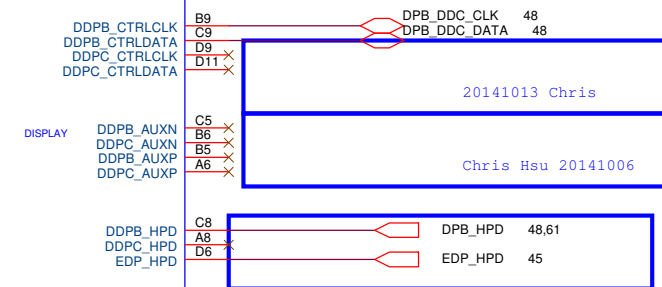
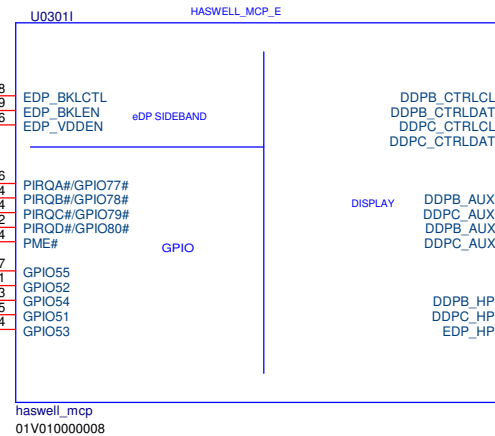
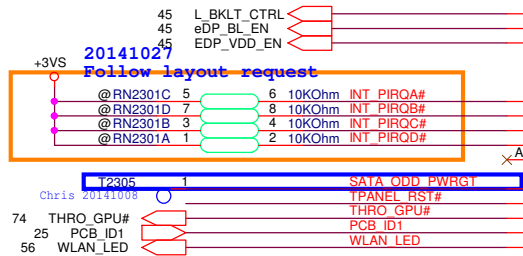
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Date: Friday, November 28, 2014 Sheet 22 of 102

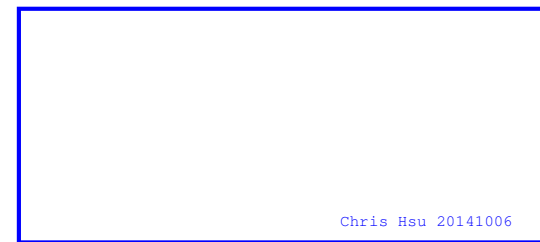
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Chris 20141015



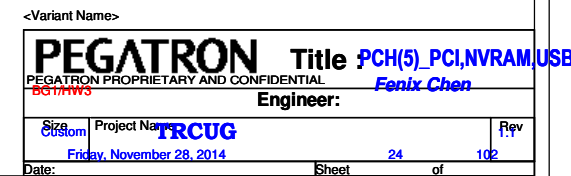
Chris 20141014



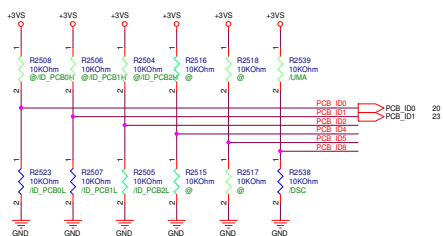
Chris Hsu 20141006

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<Variant Name>			
<b>PEGATRON</b>		Title <b>PCH(4)_DP,LVDS,CRT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL <b>Fenix Chen</b>			
BGT/HWS		Engineer:	
Size	Project Name	Rev	
8	TRCUG		
Date: Friday, November 28, 2014		Sheet 23	of 102

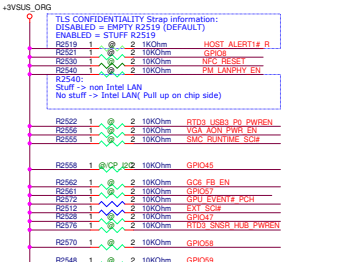
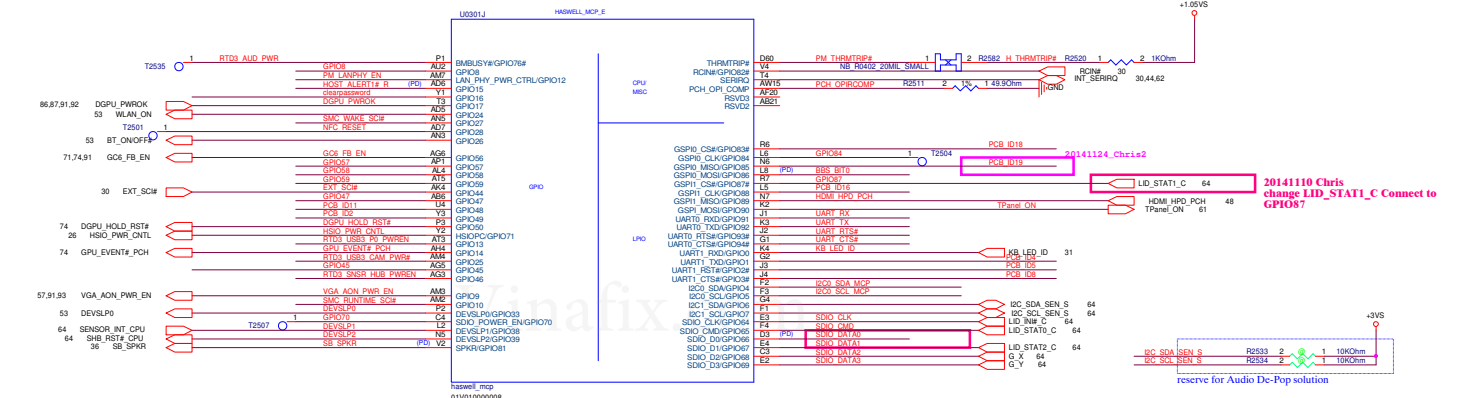
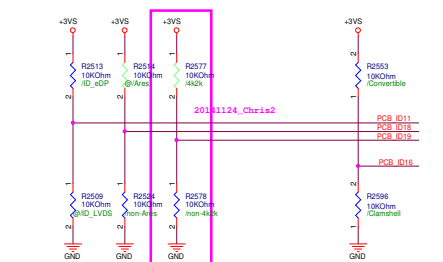




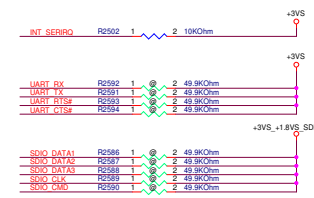
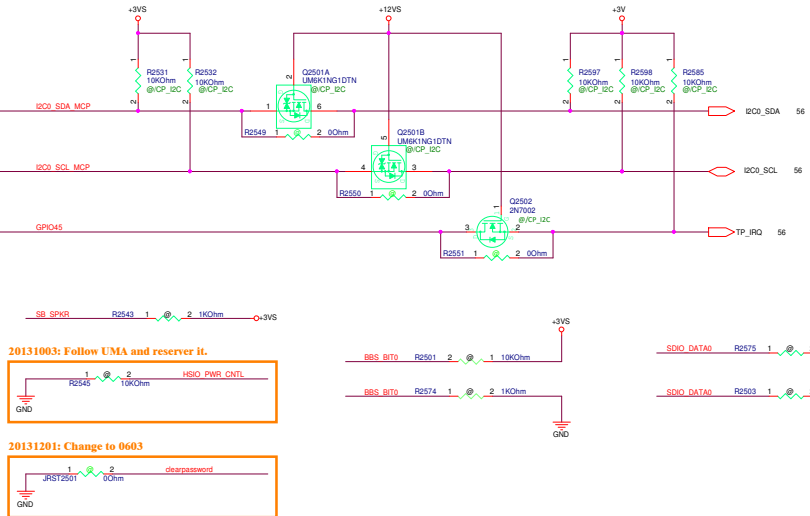
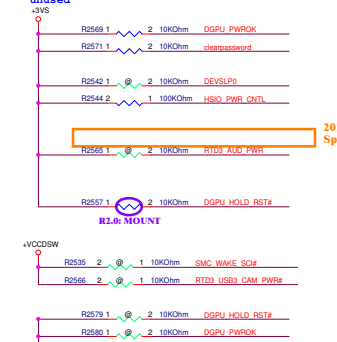


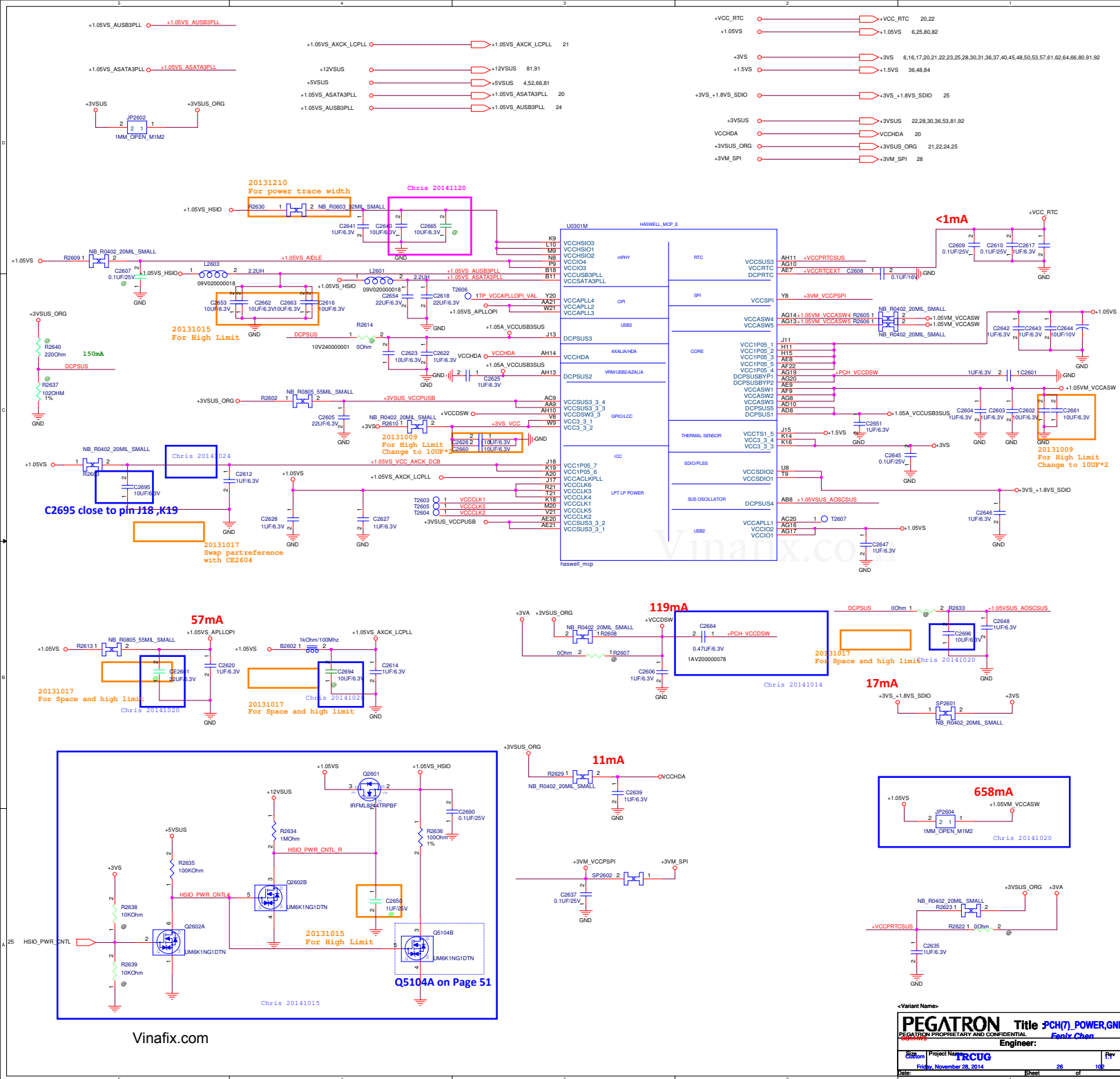
ID2	ID1	ID0	PCB Rev	ID4	ID5	USB Setting
0	0	0	R1.0	0	0	USB3*1+USB2*2
0	0	1	R1.1			
0	1	0	R2.0			
0	1	1	R2.1	0	1	USB3*2+USB2*1(1 S&C
1	0	0	TBD			
1	0	1	TBD			
1	1	0	TBD			
1	1	1	TBD			
				1	1	Reserved

PCB_ID8	PCB_ID10	PCB_ID11	PCB_ID15	PCB_ID16	PCB_ID18	PCB_ID19	KB_LED_ID	ONKYO_DET	HARMAN_DET
1: UMA	1: S&C_ID	1: eDP	1: TP_SMB	1: Convertible	1: Ares	1: 4k2k	1: W/O KB LED	1: W/O ONKYO	1: W/O HARMAN
0: DSC	0: Non_S&C_ID	0: LVDS	0: TP_PS2	0: Clamshell	0: Non-Ares	0: non-4k2k	0: W/ KB LED	0: W/ ONKYO	0: W/ HARMAN



GPIO need to pull high to power with 10Kohm if unused

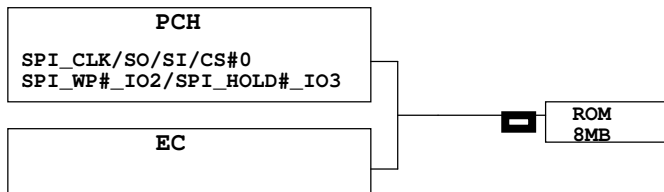
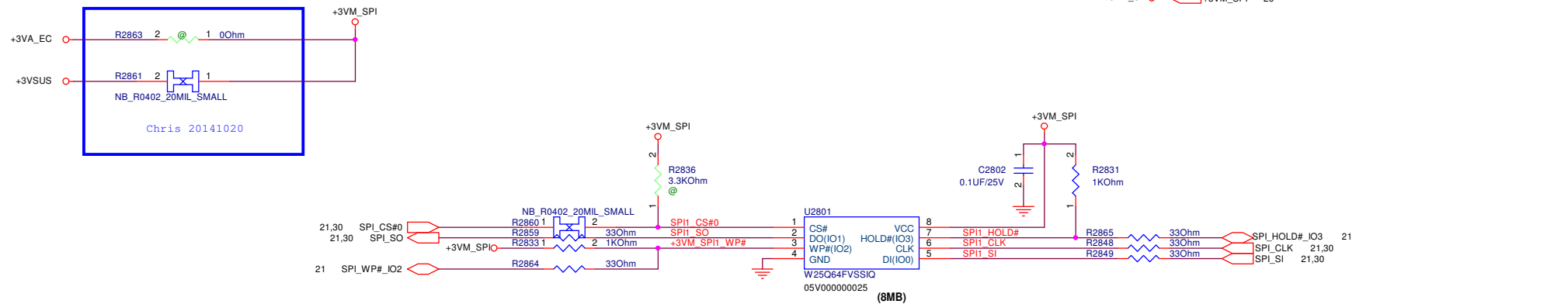




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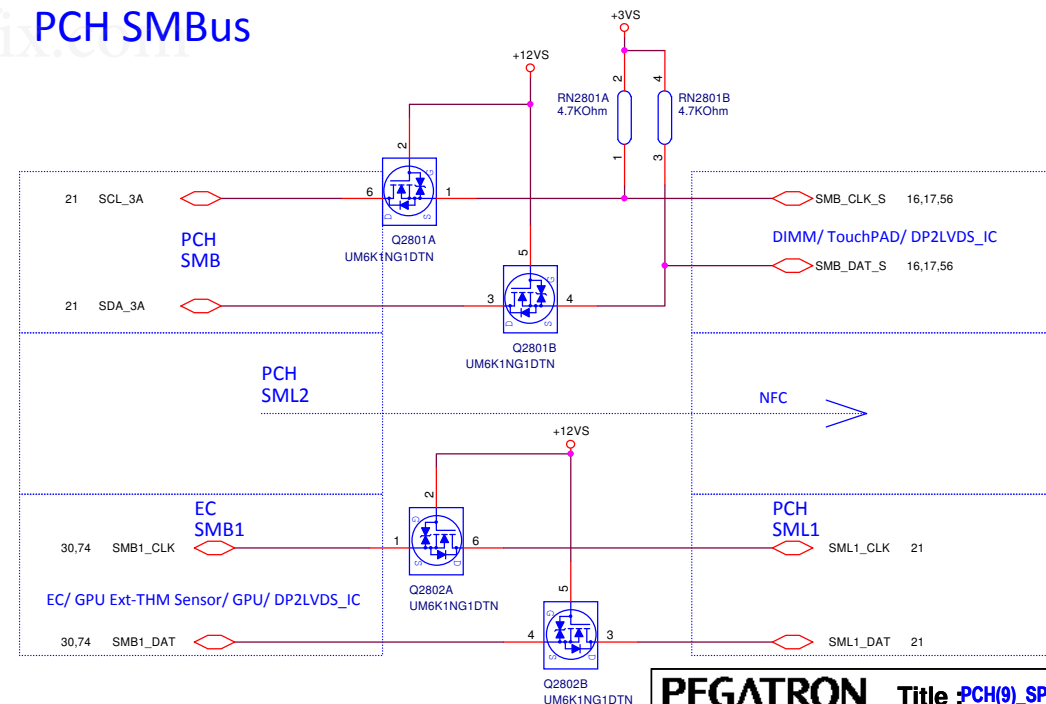
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer:</b>	
Size	Project Name		Rev.
	Friday, November 28, 2014	1	27 of 102
Date Sheet of			

# PCH SPI ROM



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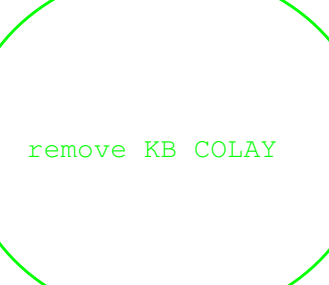
# PCH SMBus



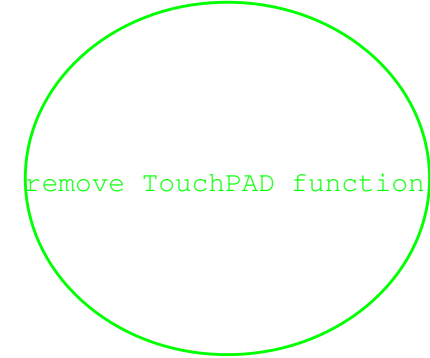

5	4	3	2	1					
D					D				
C					C				
B					B				
A					A				
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					<div>&lt;Title&gt;</div> <div>Engineer:</div>				
					<table><tr><td>Size A</td><td>Project Name</td><td>TRCUG</td><td>Rev 1.0</td></tr></table>	Size A	Project Name	TRCUG	Rev 1.0
Size A	Project Name	TRCUG	Rev 1.0						
					<div>Date: Friday, November 28, 2014</div> <div>Sheet 29 of 102</div>				
5	4	3	2	1					

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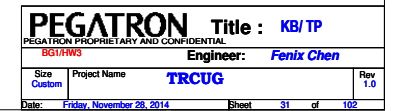


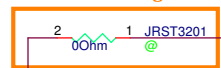


remove KB COLAY

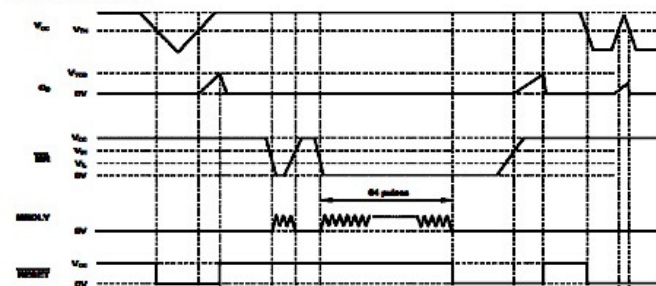
[illegible][illegible]

Changed Click PAD Function





### Timing Diagram

[illegible]

**Design for Pull low the "RTC\_RST" and "EC\_RST" at same time.**

<Variant Name>

PEGATRON Title : RST\_Reset Circuit

PEGATRON PROPRIETARY AND CONFIDENTIAL  
BG1/HW3 Engineer: Fenix Chen

Size B	Project Name <b>TRCUG</b>	Rev 1.0
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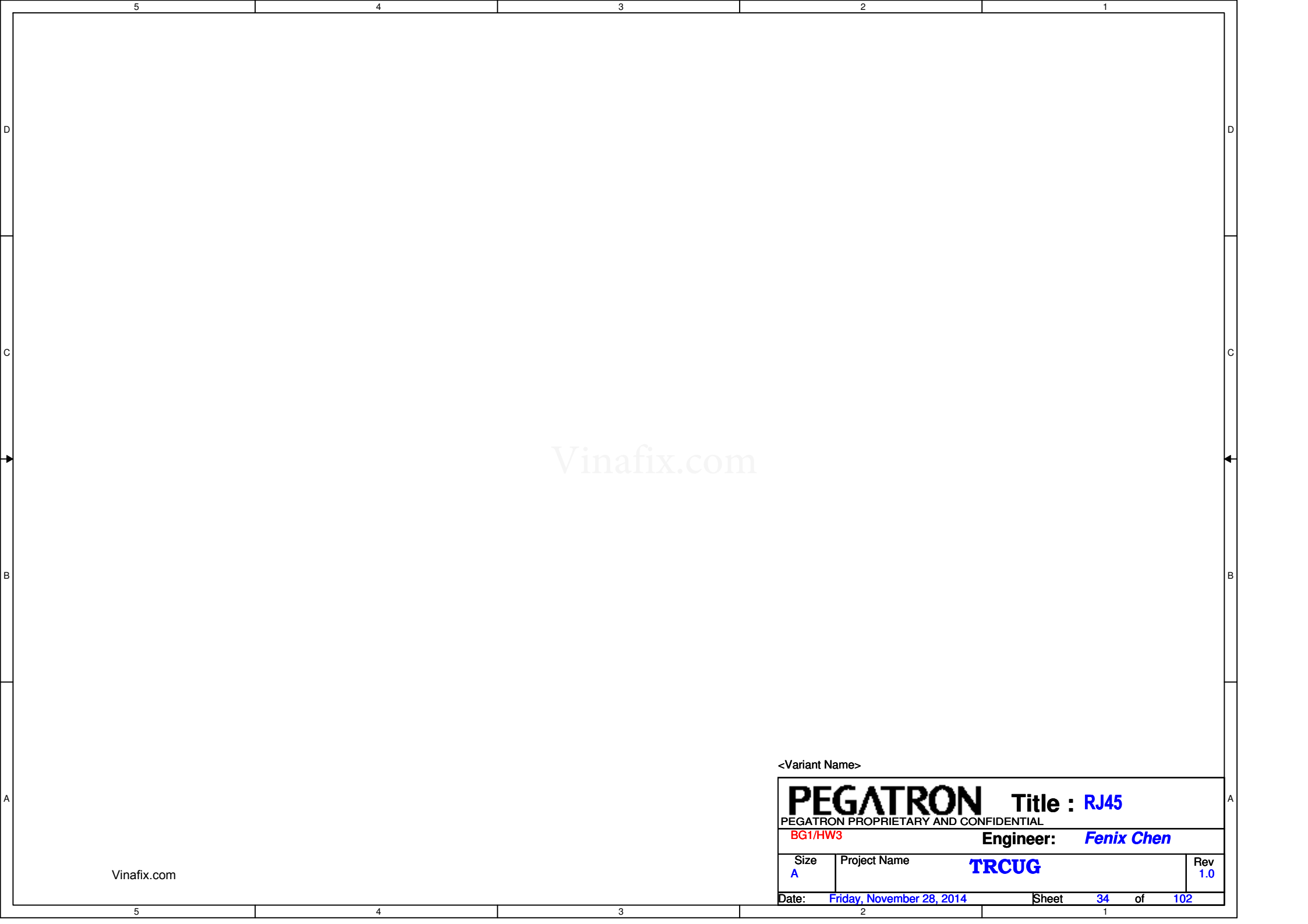


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<Variant Name>

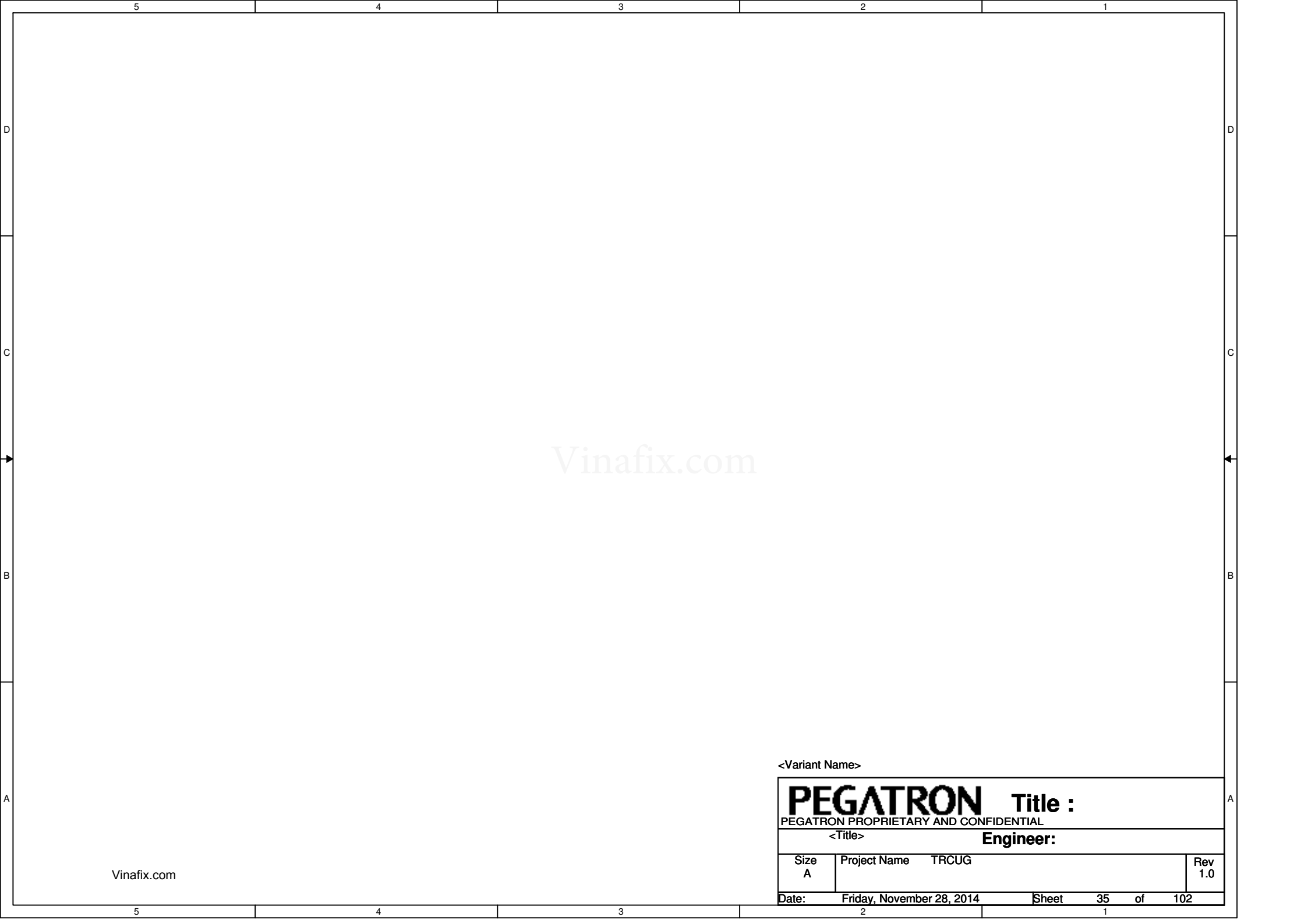
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PEGATRON PROPRIETARY AND CONFIDENTIAL		
<b>BG1/HW3</b> Engineer: <b>Fenix Chen</b>		
Size Custom	Project Name <b>TRCUG</b>	Rev 1.0
Date: <b>Friday, November 28, 2014</b>		Sheet <b>33</b> of <b>102</b>



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<Variant Name>

<b>PEGATRON</b>		Title : <b>RJ45</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Fenix Chen</b>	
Size <b>A</b>	Project Name <b>TRCUG</b>		Rev <b>1.0</b>
Date: <b>Friday, November 28, 2014</b>		Sheet <b>34</b> of <b>102</b>	

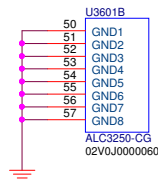


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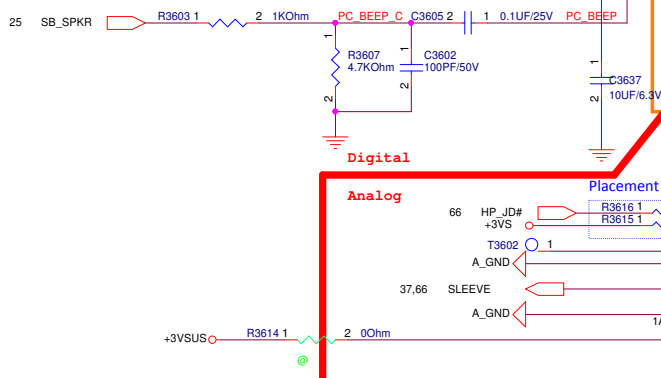
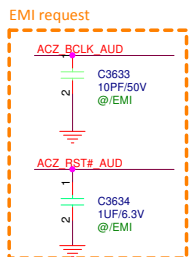
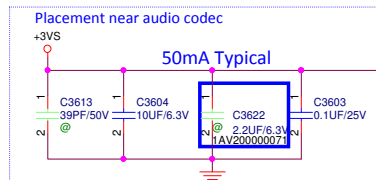
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<b>PEGATRON</b> Title :			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size A	Project Name TRCUG		Rev 1.0
Date:	Friday, November 28, 2014	Sheet	35 of 102



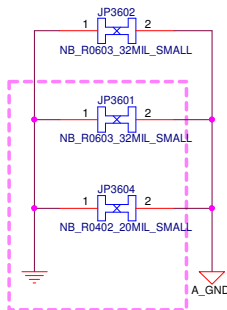
20131204:  
Must check VIA!!

20131203:  
For 3 POLE MIC ,  
Change from  
ALC269 to ALC 233



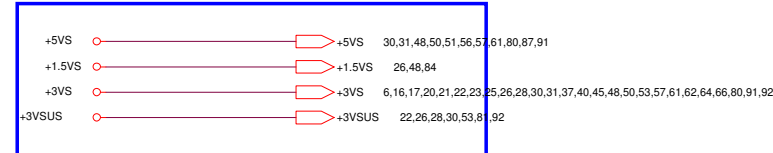
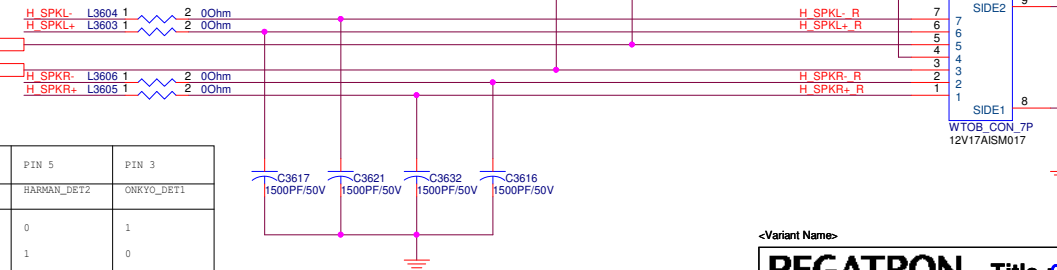
### Configuration for ALC233

Internal Speaker: Port D  
External Headphone: Port A  
3 POLE Microphone: LINE 1  
Digital Microphone: Pin2,3

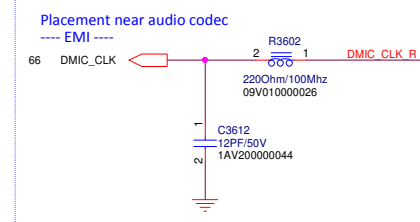
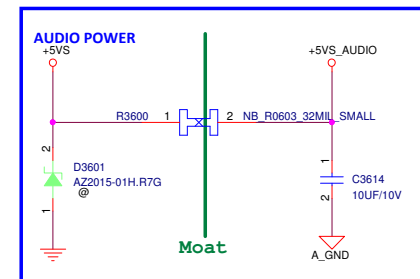


20140214 change to short pin.  
need to verify with EMI/ESD needed

Speaker Pin	PIN 5	PIN 3
Schematic Pin	HARMAN_DET2	ONKYO_DET1
Harman Kardon	0	1
Onkyo	1	0
No Brand	1	1
Reserved	0	0



20141024 Chris



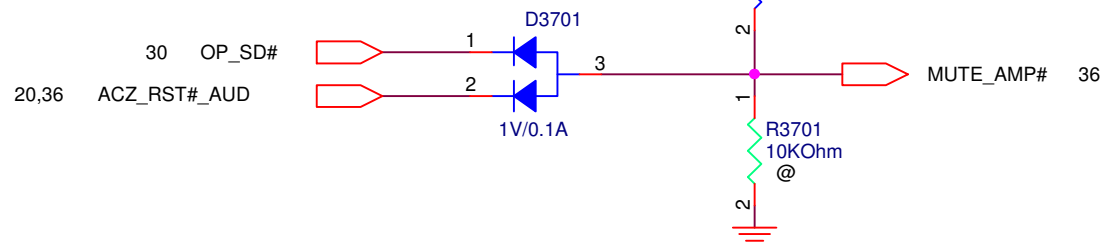
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**PEGATRON** Title :CODEC-ALC233  
PEGATRON PROPRIETARY AND CONFIDENTIAL Mike Pan

Size 801/HW3 Project Name: TRCUG Engineer:

Date: Friday, November 28, 2014 Sheet 36 of 99

# AMP De-Pop Control circuit

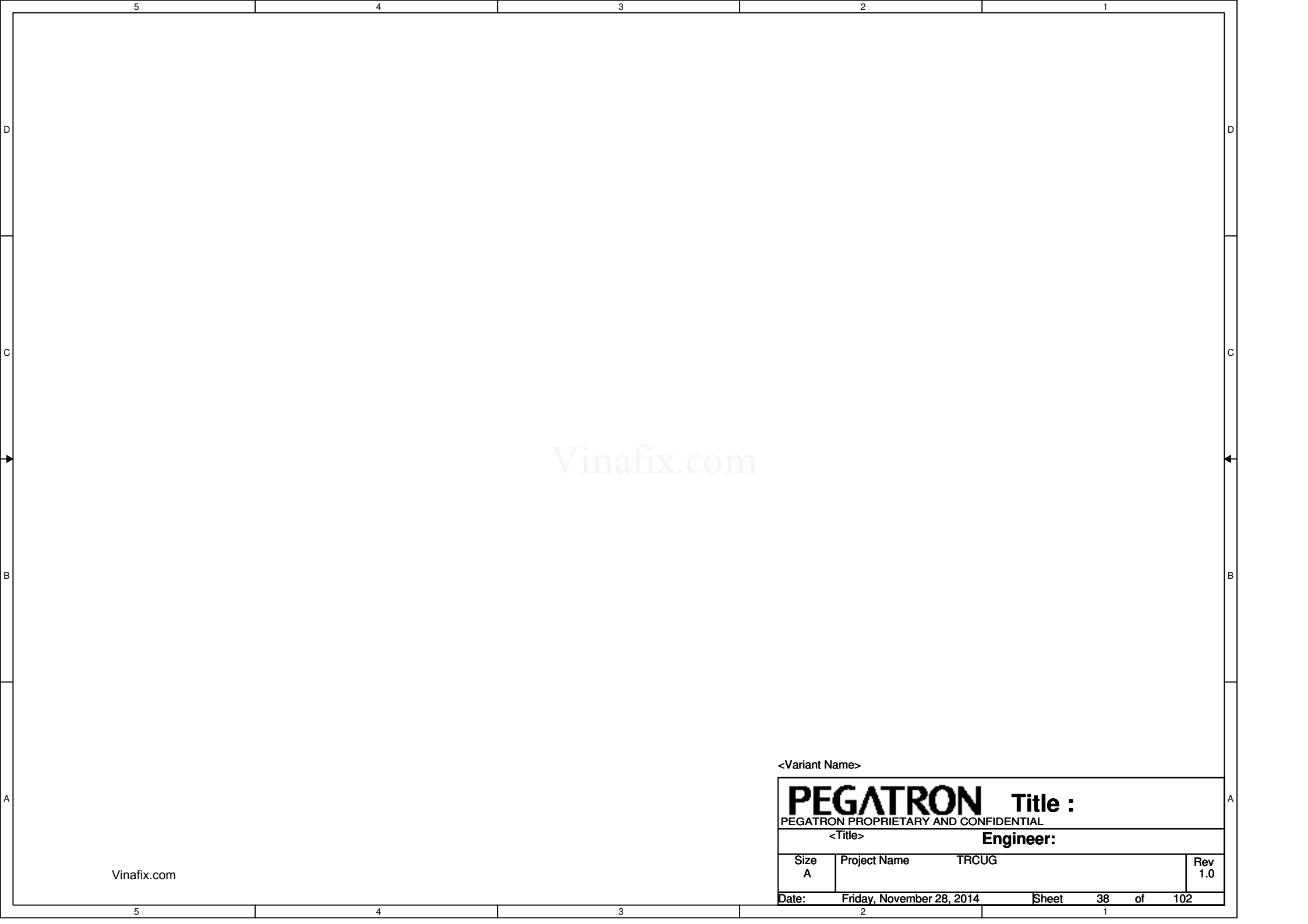


20131203: For 3 Pole MIC

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<Variant Name>

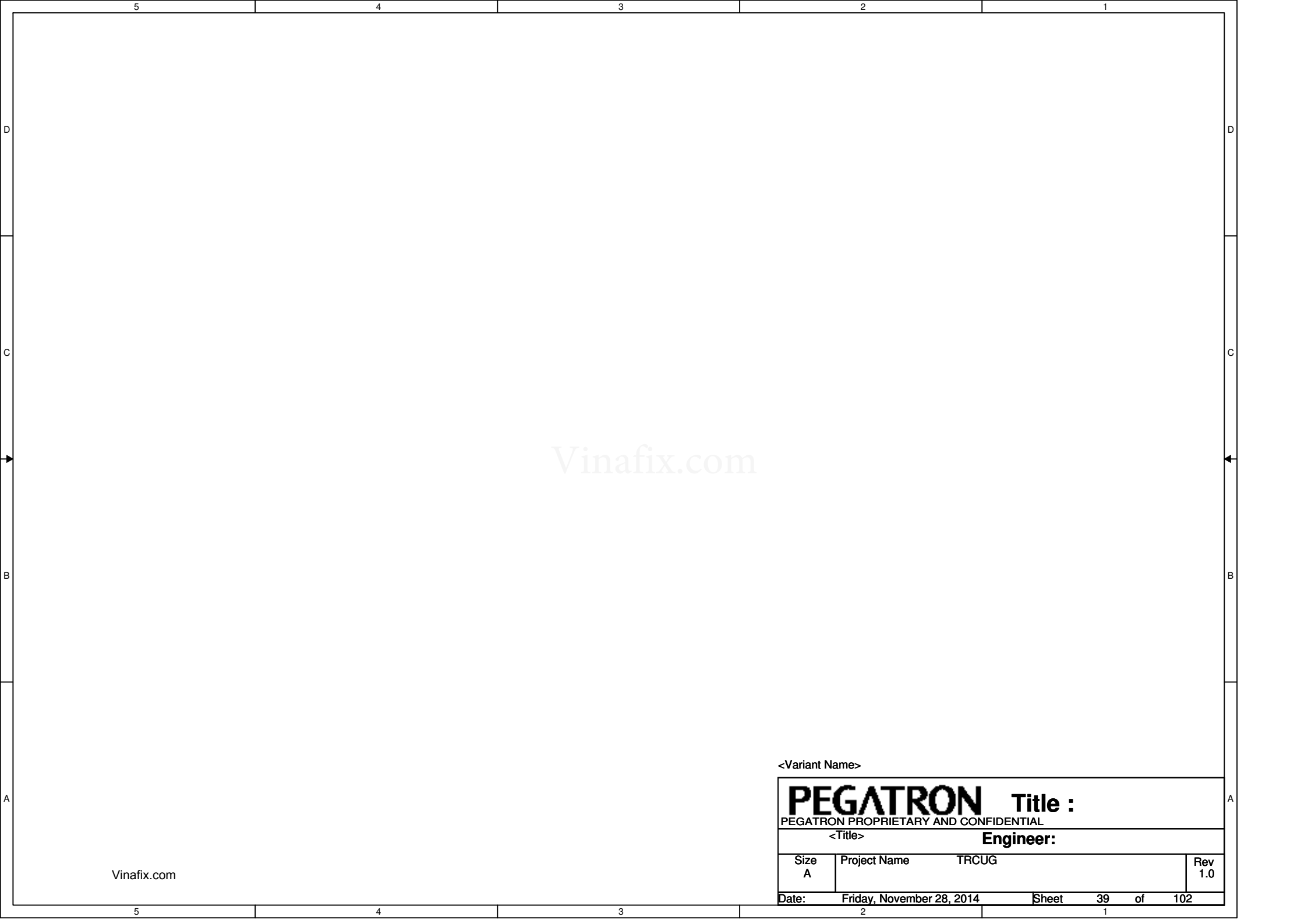
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Mike Pan</b>	
Size <b>A</b>	Project Name <b>TRCUG</b>		Rev <b>1.0</b>
Date: <b>Friday, November 28, 2014</b>	Sheet <b>37</b> of <b>102</b>		



Vinafix.com

<Variant Name>

<b>PEGATRON</b> Title :			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size A	Project Name TRCUG		Rev 1.0
Date:	Friday, November 28, 2014	Sheet	38 of 102

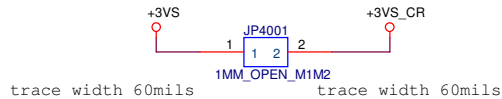


Vinafix.com

<Variant Name>

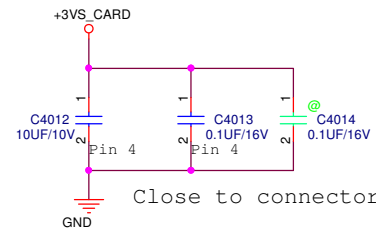
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size A	Project Name	TRCUG	Rev 1.0
Date:	Friday, November 28, 2014	Sheet	39 of 102

## Power Source



20	PCIE_TXP_CR	PCIE_TXP_CR
20	PCIE_TXN_CR	PCIE_TXN_CR
20	PCIE_RXP_CR	PCIE_RXP_CR
20	PCIE_RXN_CR	PCIE_RXN_CR
21	CLK_PCIE_CR_PCH	CLK_PCIE_CR_PCH
21	CLK_PCIE_CR#_PCH	CLK_PCIE_CR#_PCH
21	CLK_CR_REQ#	CLK_CR_REQ#
22,30,53,62,74	BUF_PLT_RST#	BUF_PLT_RST#

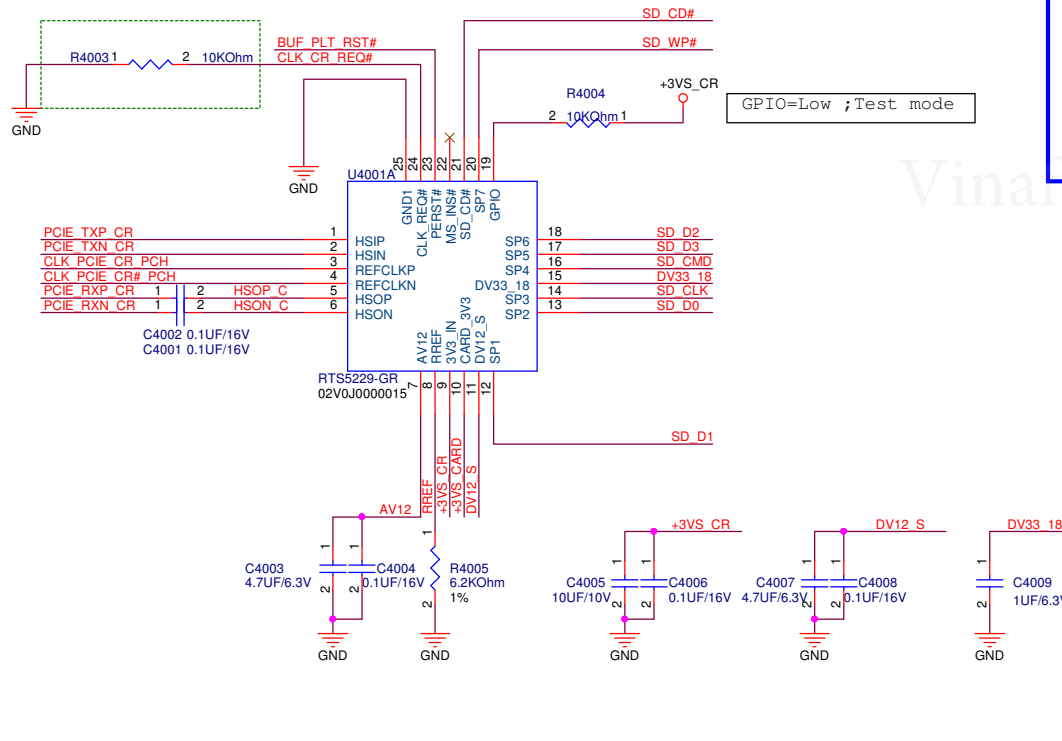
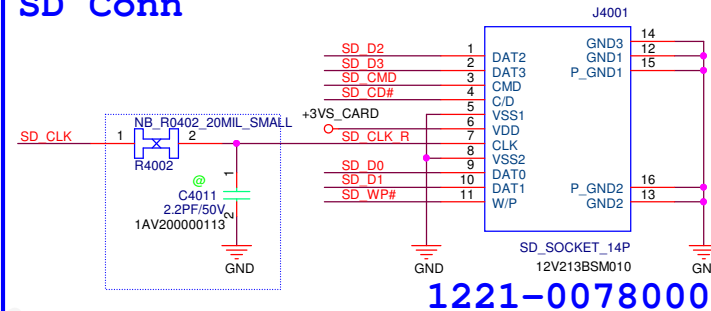
## SD Power



+3VS 6,16,17,20,21,22,23,25,26,28,30,31,36,37,45,48,50,53,57,61,62,64,66,80,91,92

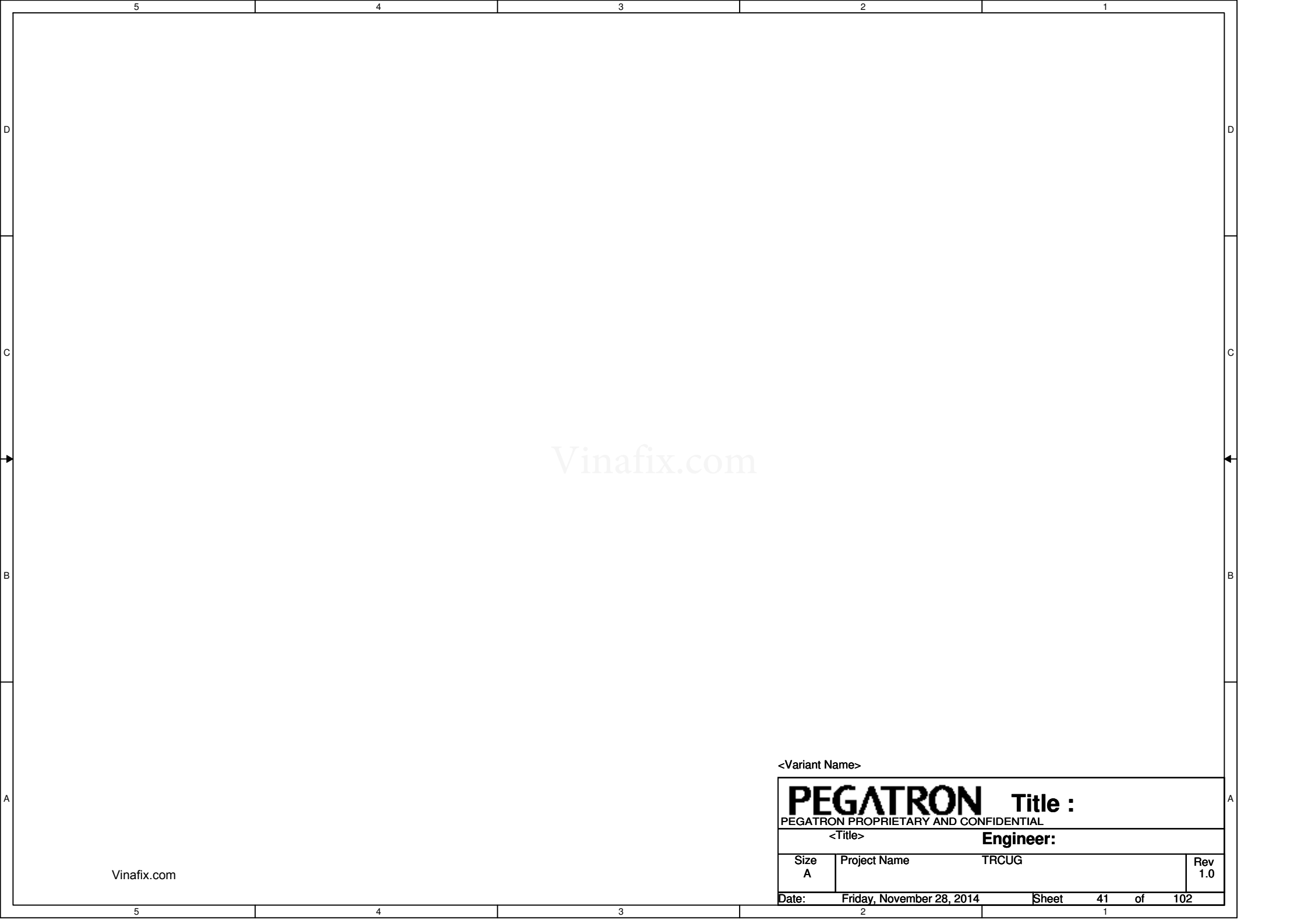
20141024 Chris

## SD Conn



<b>PEGATRON</b>		Title : CardReader RTS5229	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Raly Hsieh	
Size B	Project Name <b>TRCUG</b>		Rev 1.0
Date: Friday, November 28, 2014	Sheet 40 of 102		

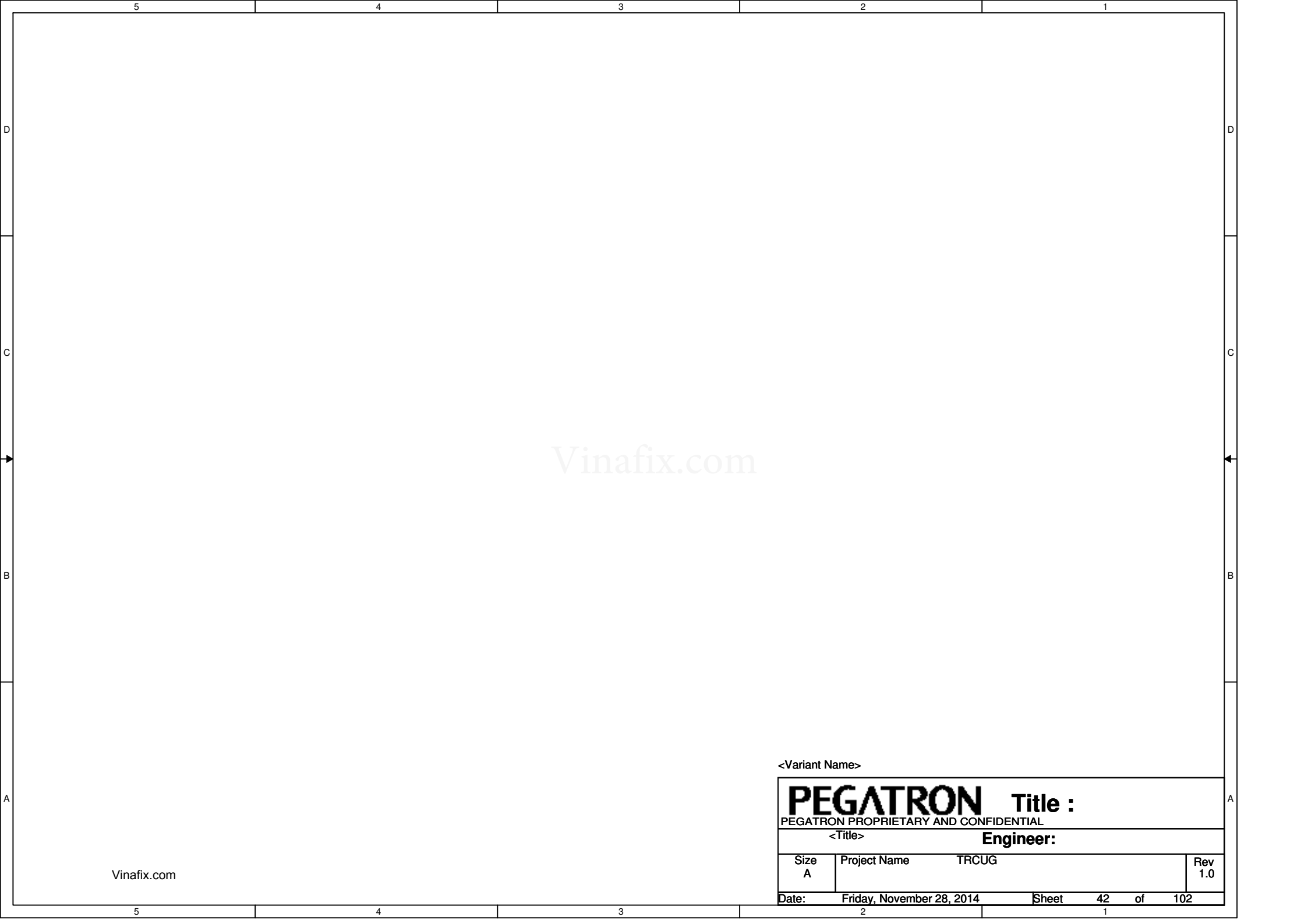




Vinafix.com

<Variant Name>

<b>PEGATRON</b> Title :			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size A	Project Name	TRCUG	Rev 1.0
Date:	Friday, November 28, 2014	Sheet	41 of 102

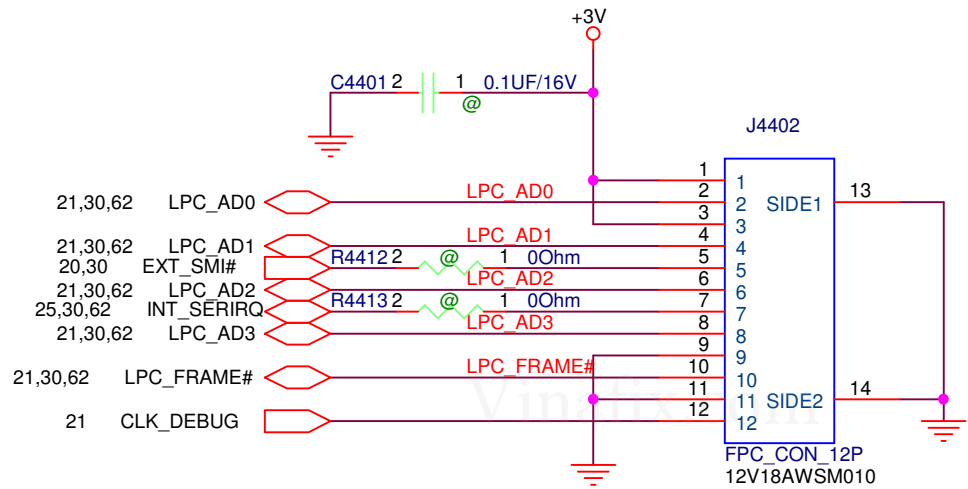


Vinafix.com

<Variant Name>

<b>PEGATRON</b> Title :			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size A	Project Name TRCUG		Rev 1.0
Date:	Friday, November 28, 2014	Sheet	42 of 102

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D					D				
C					C				
B					B				
A					A				
					<Variant Name>				
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					PEGATRON PROPRIETARY AND CONFIDENTIAL				
					<div>&lt;Title&gt;</div> <div>Engineer:</div>				
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Size A	Project Name	TRCUG	Rev 1.0						
					<div>Date: Friday, November 28, 2014</div> <div>Sheet 43 of 102</div>				

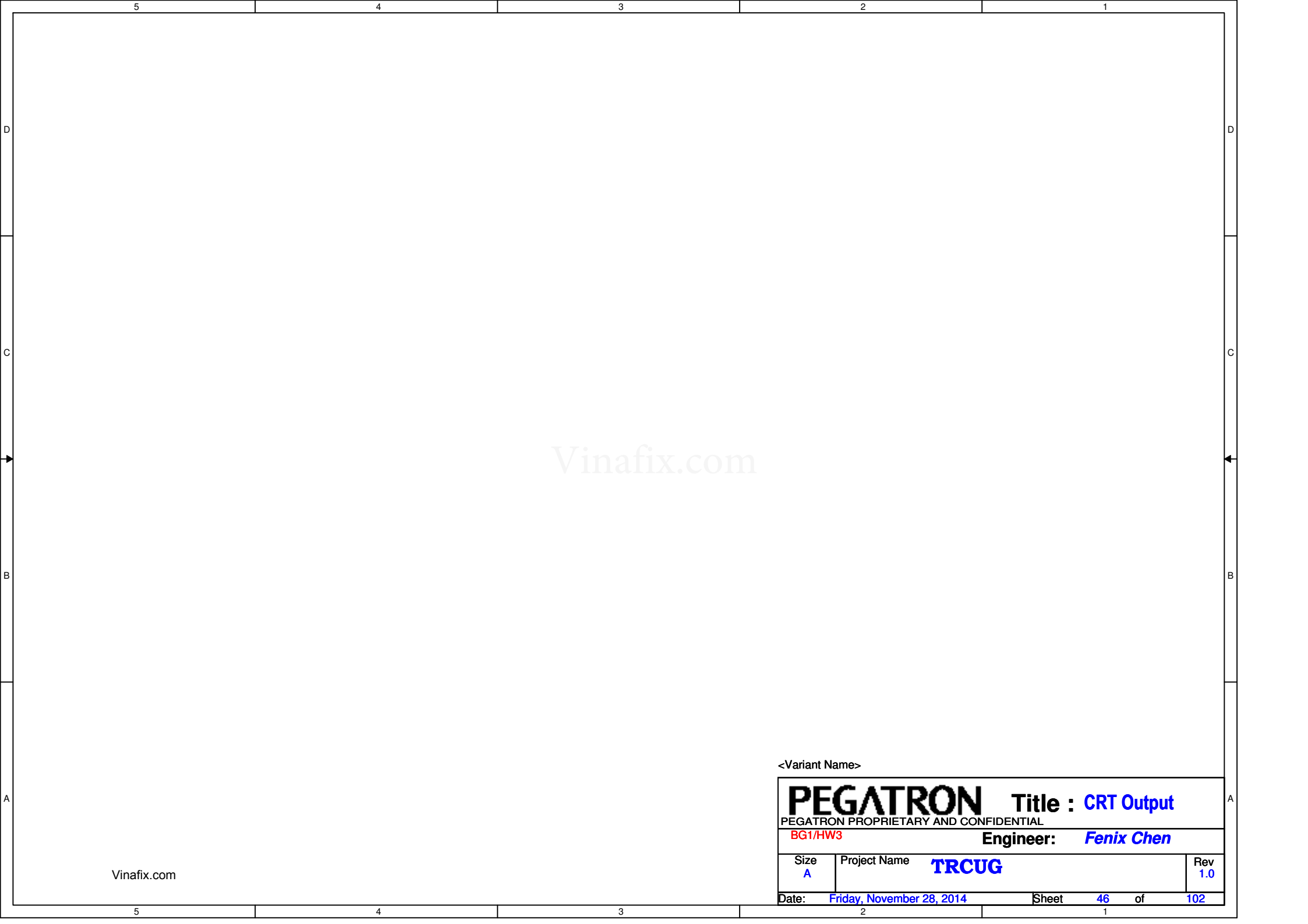


Vinafix.com

<Variant Name>

<b>PEGATRON</b>		Title : <b>BUG_Debug</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Fenix Chen</b>	
Size <b>A</b>	Project Name <b>TRCUG</b>		Rev <b>1.0</b>
Date: <b>Friday, November 28, 2014</b>		Sheet <b>44</b> of <b>102</b>	



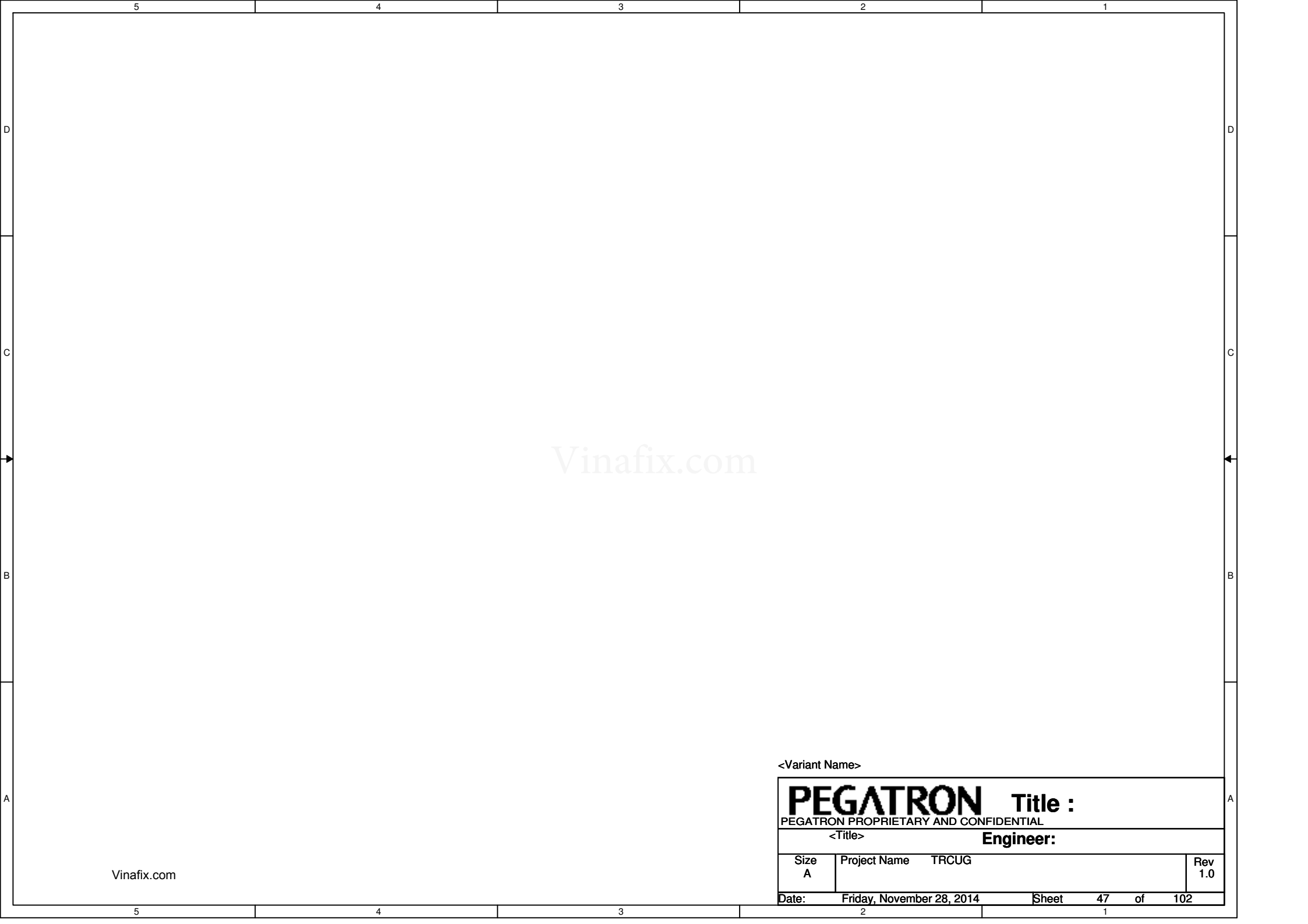


Vinafix.com

Vinafix.com

<Variant Name>

<b>PEGATRON</b>		<b>Title :</b> CRT Output	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer:</b> Fenix Chen	
Size A	Project Name TRCUG		Rev 1.0
Date:	Friday, November 28, 2014	Sheet	46 of 102



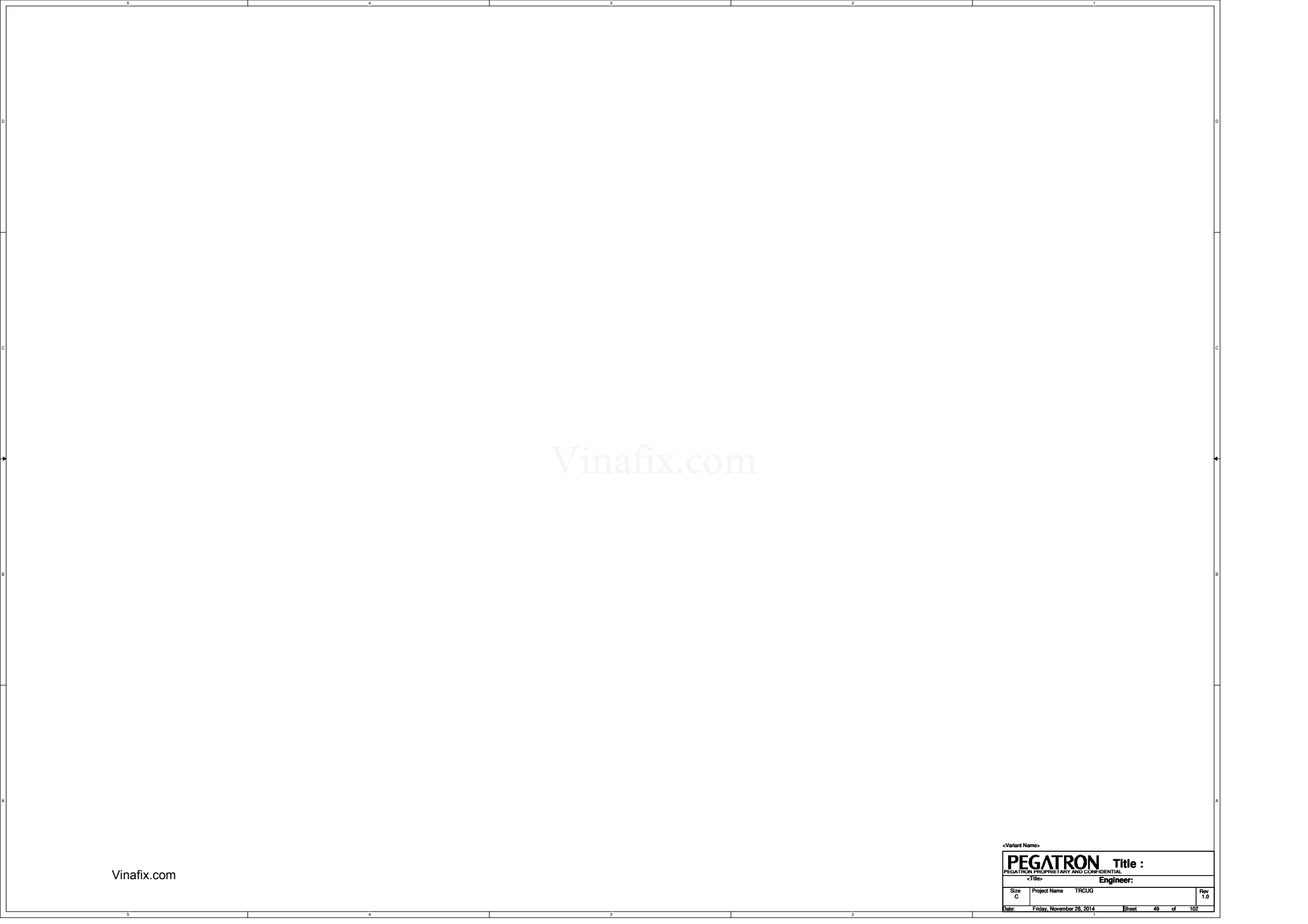
Vinafix.com

<Variant Name>

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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size A	Project Name TRCUG		Rev 1.0
Date:	Friday, November 28, 2014	Sheet	47 of 102



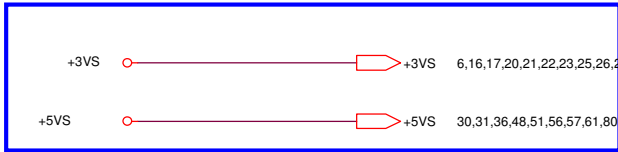




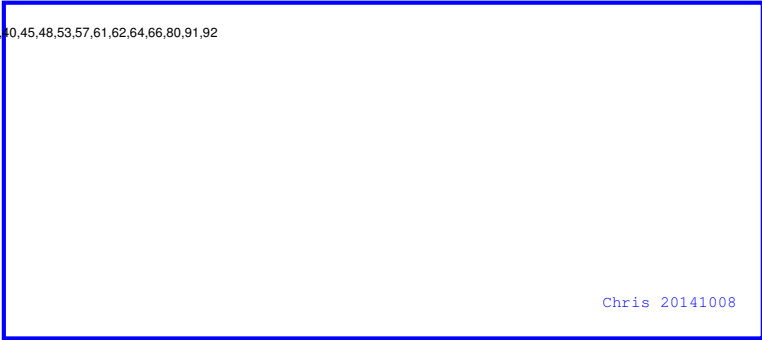
Vinafix.com

Vinafix.com

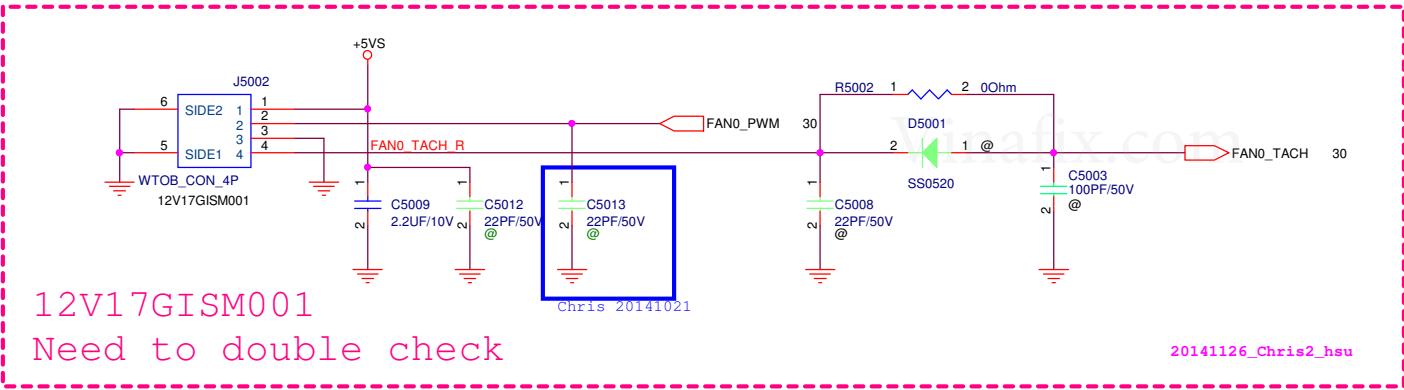
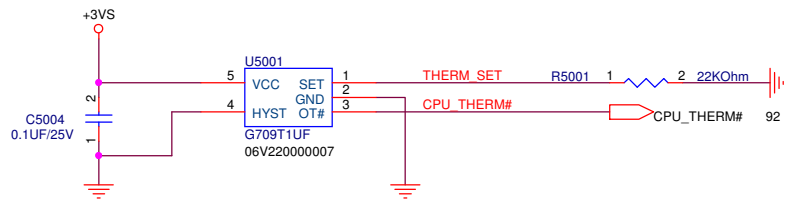
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		<b>Engineer:</b>	
Size C	Project Name TRCUG	Rev 1.0	
Date: Friday, November 28, 2014		Sheet 49 of 102	



20141024 Chris



Chris 20141008

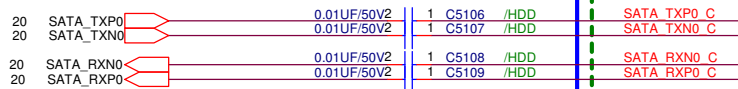


12V17GISM001  
Need to double check

Chris 20141021

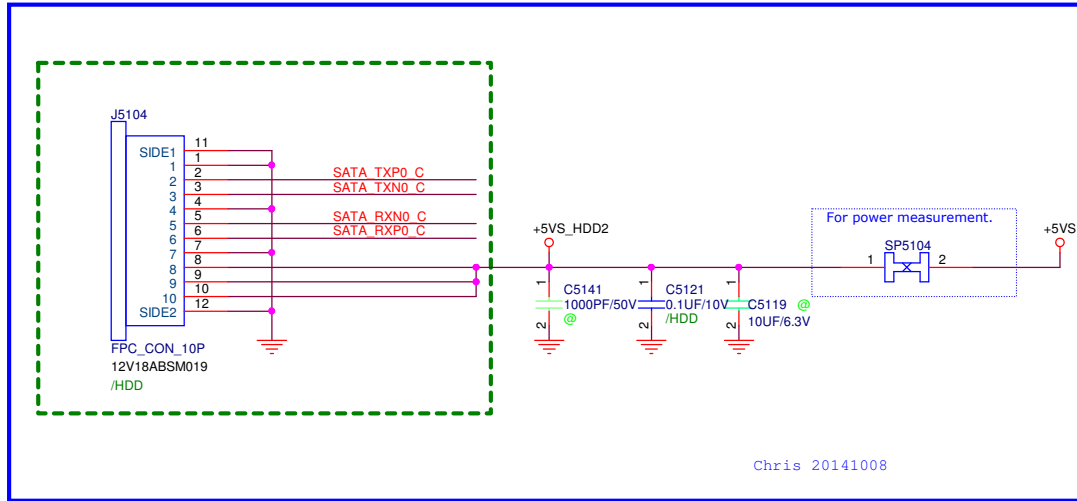
20141126\_Chris2\_hsu

<b>PEGATRON</b>		Title : <b>THERMAL/ FAN</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>BG1/HW3</b>		Engineer: <b>Fenix Chen</b>	
Size B	Project Name <b>TRCUG</b>		Rev 1.0
Date: <b>Friday, November 28, 2014</b>		Sheet <b>50</b>	of <b>102</b>



+5VS 30,31,36,48,50,56,57,61,80,87,91

20141024 Chris



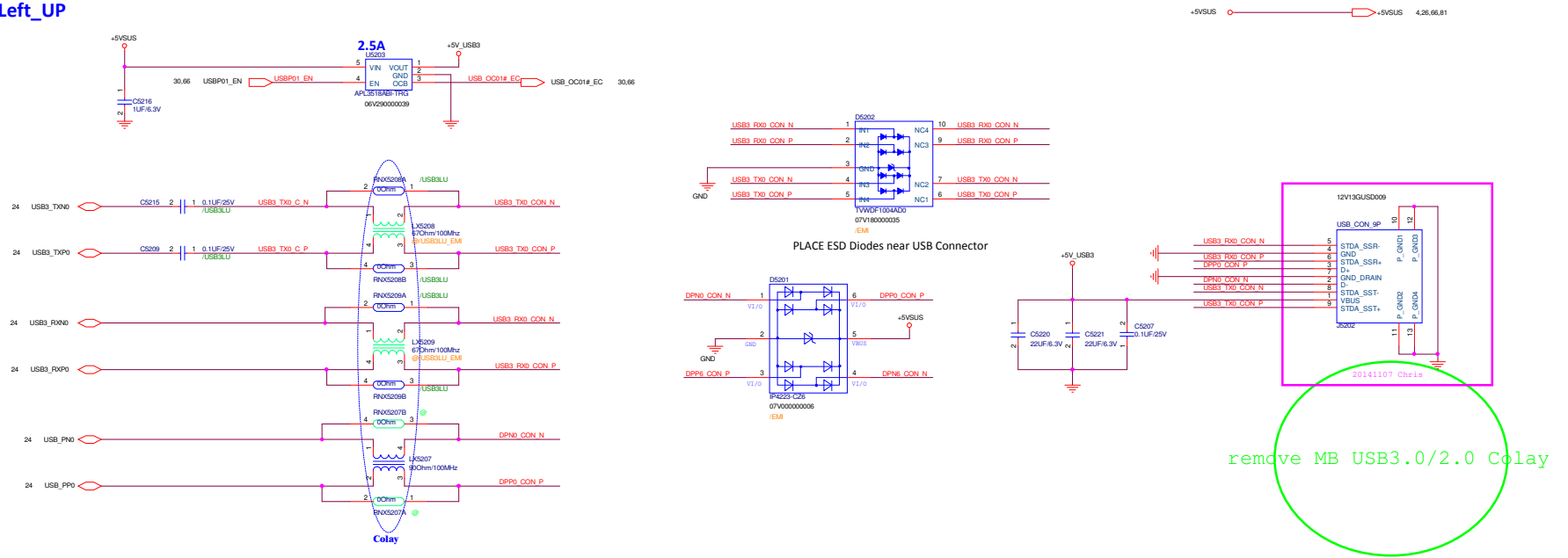
Chris 20141008

For ME request for use same cable with Z710

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<b>PEGATRON</b>		Title : SATA HDD/ ODD	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer:	
Size B	Project Name <b>TRCUG</b>		Rev 1.0
Date: Friday, November 28, 2014		Sheet	51 of 102

## USB 3.0 (USB 2.0 colay) ports x 1 Left\_UP



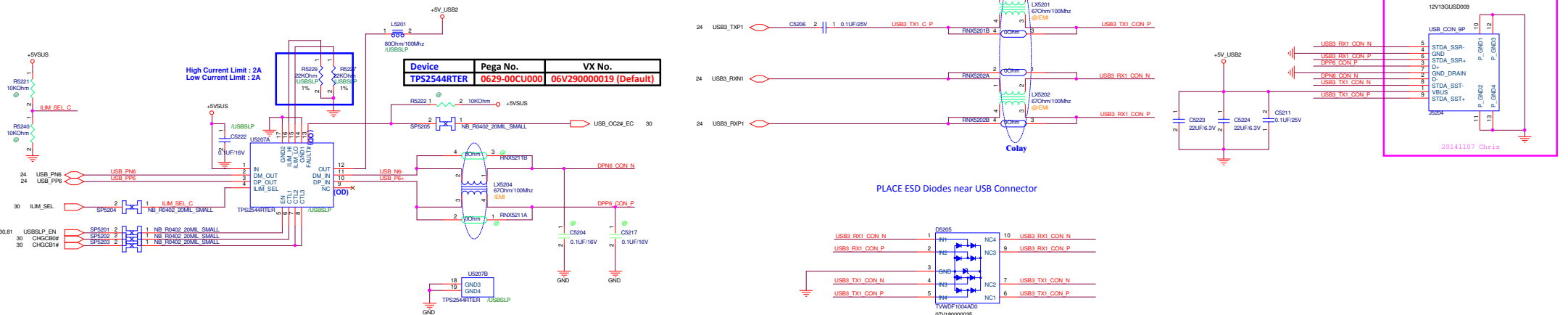
## USB 3.0 ports x 1 with Sleep & Charge Left\_Down

TPS2544 Device True Table

Sleep & Charge Function Setting	State	Charging Mode	Wake up	CHGCB0#	CHGCB1#	ILIM_SEL	USBLP_EN	Backup
Auto Mode	S0	CDP	NA	1	1	1	1	Wake up by KB/MS at S3 state
	S3~S5	DCP Auto	NA	0	1	1	1	
Alternative Mode	S0	CDP	NA	1	1	1	1	Wake up by KB/MS at S3 state
	S3~S5	DCP Auto	NA	0	1	1	1	
Disable	S0	CDP	NA	1	1	1	1	Wake up by KB/MS at S3 state
	S3	SDP	Enable wake up	1	1	0	1	
	S3	Discharge	Disable wake up	1	1	0	0	
	S4/S5	Discharge	NA	0	0	1	0	

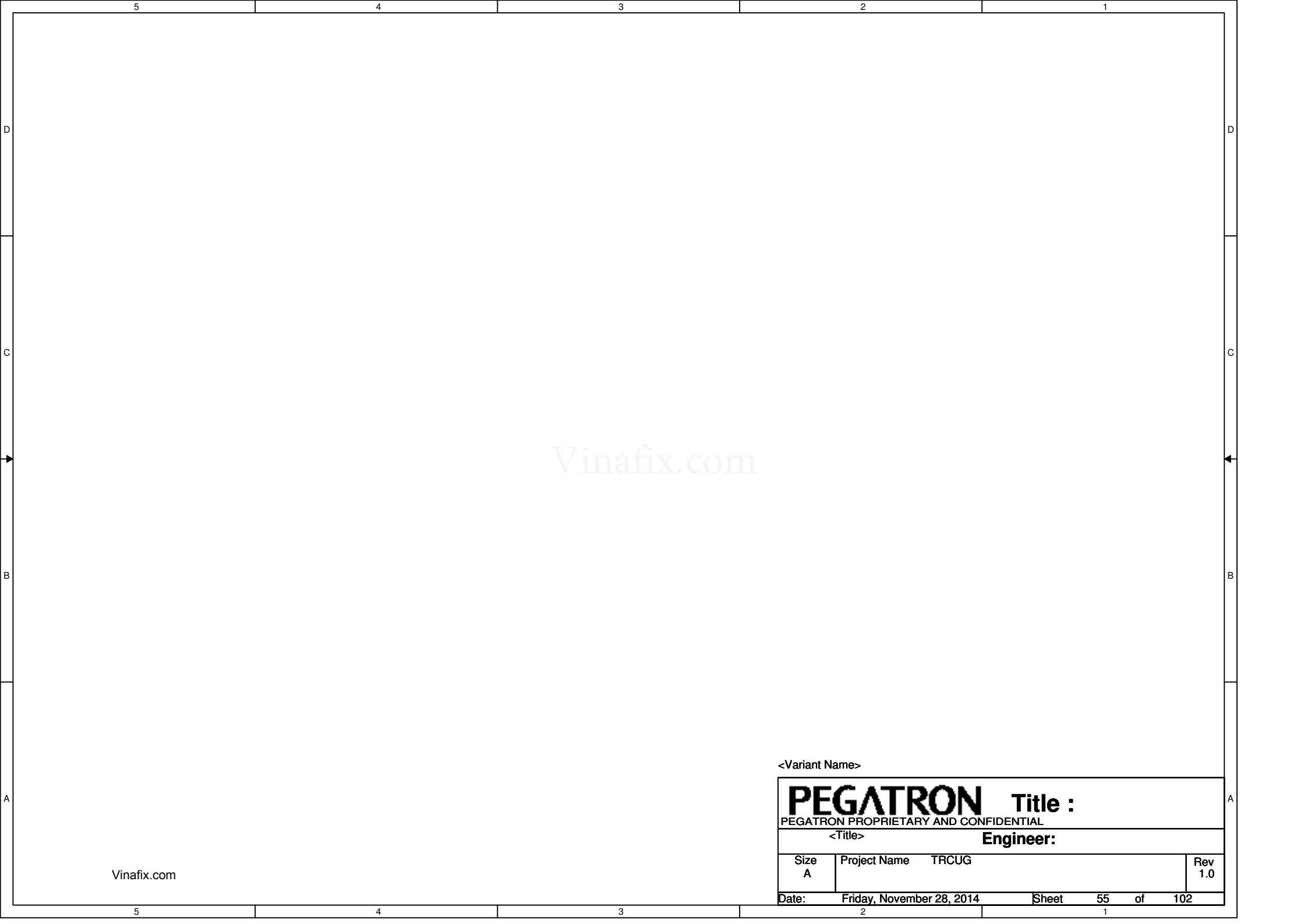
### Tod's spec

Battery Charge mode	
Apple 1.0A mode	Yes
DCP mode	Yes
Apple 2.0A mode	Yes



Vinafix.com

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D					D
C					C
B					B
A					A
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<div><div>&lt;Title&gt;</div><div>Engineer:</div></div>					
<div><div><div>Size A</div><div>Project Name TRCUG</div><div>Rev 1.0</div></div></div>					
<div><div>Date: Friday, November 28, 2014</div><div>Sheet 54 of 102</div></div>					
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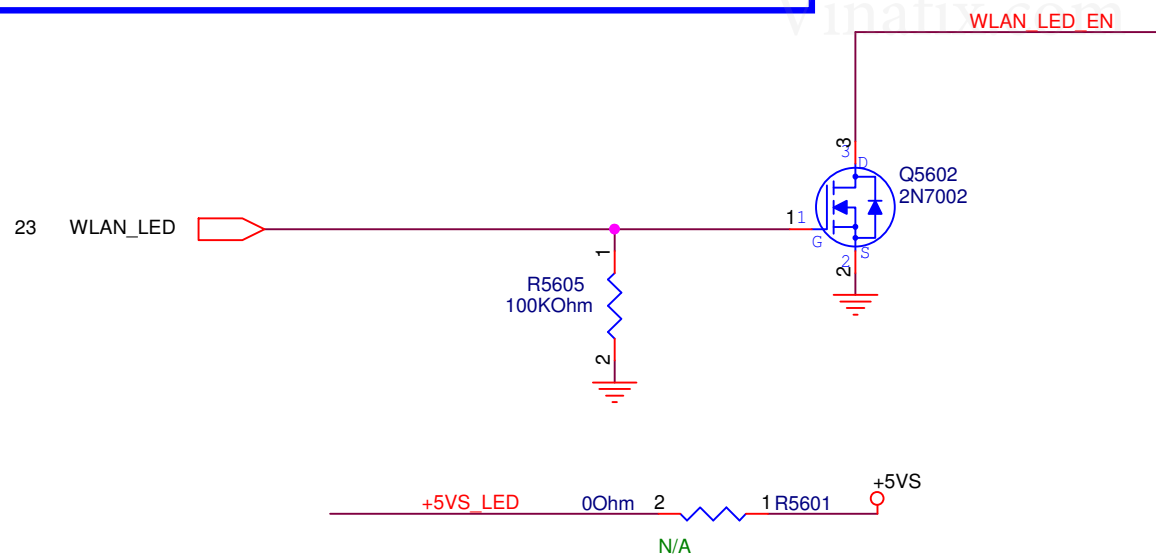
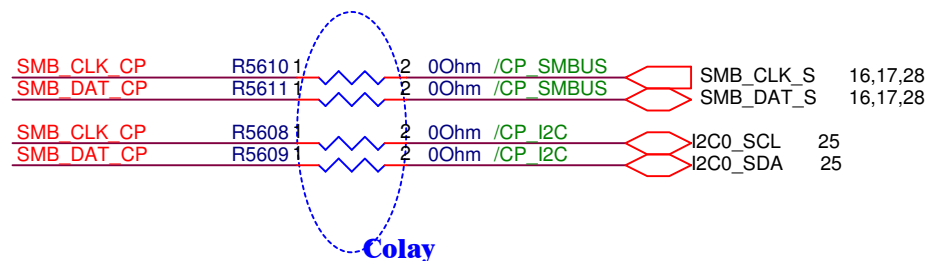
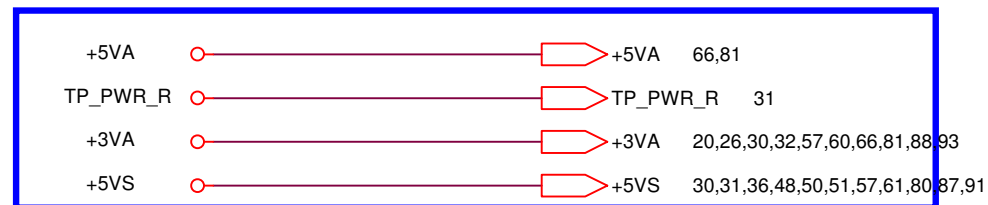
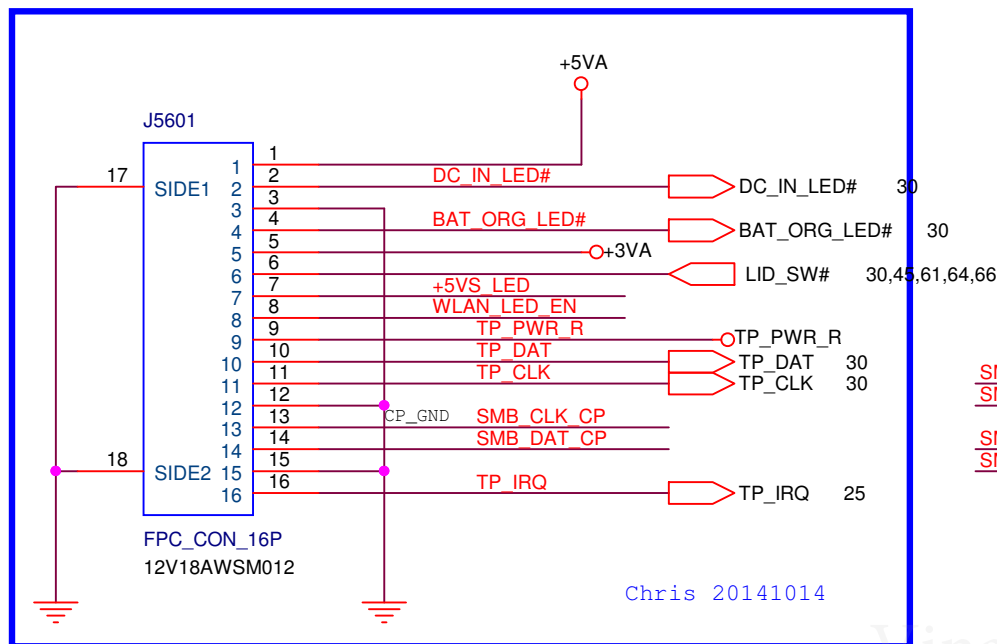
Vinafix.com

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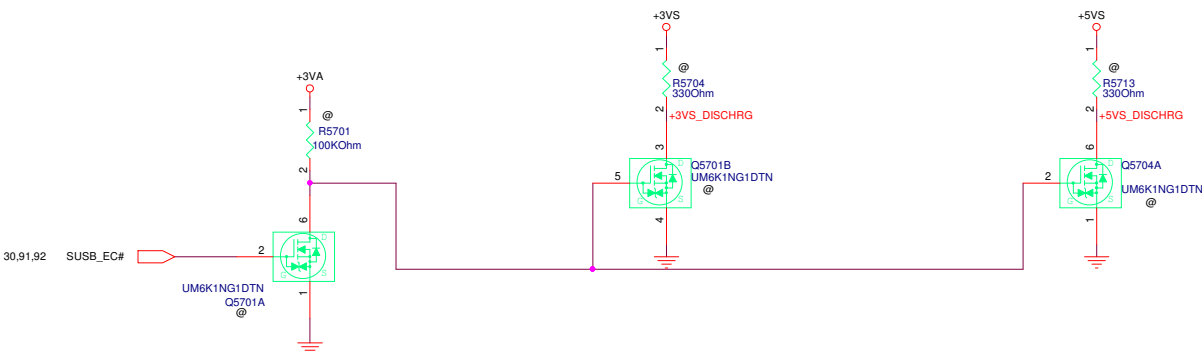
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size A	Project Name TRCUG		Rev 1.0
Date:	Friday, November 28, 2014	Sheet	55 of 102

# LED BD 16pin: include LED/Click PAD Function



<b>PEGATRON</b>		<b>Title :</b> LED	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		<b>Engineer:</b> Fenix_Chen	
Size A	Project Name <b>TRCUG</b>		Rev 0.5
Date: Friday, November 28, 2014		Sheet 56 of 102	



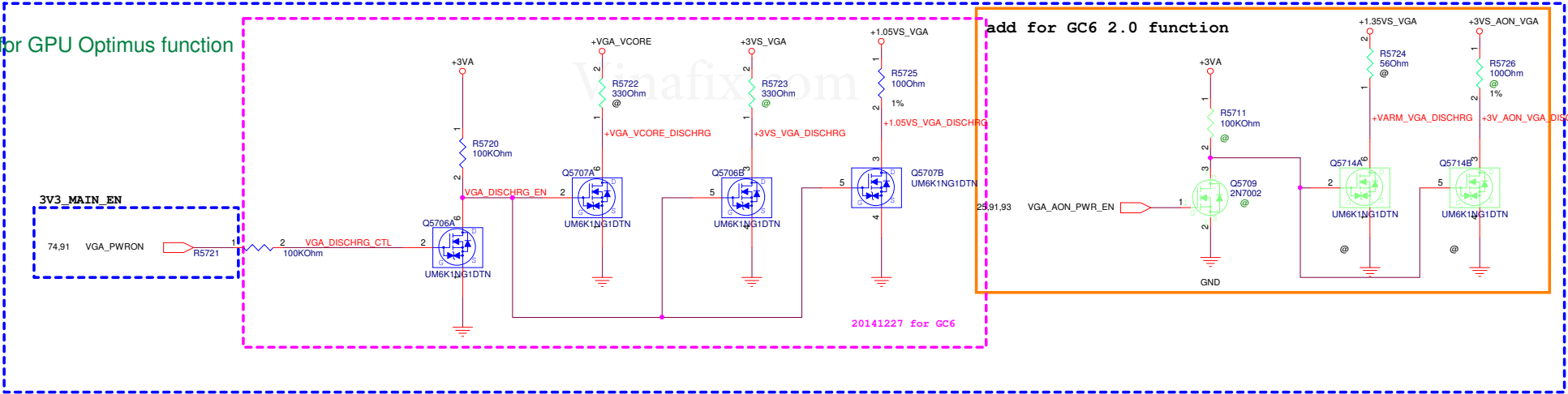


+3VA	20,26,30,32,56,60,66,81,88,93
+3VS	6,16,17,20,21,22,23,25,26,28,30,31,36,37,40,45,48,50,53,61,62
+3VS_AON_VGA	70,72,74,75,91
+1.35VS_VGA	71,75,76,77,91
+1.05VS_VGA	70,71,72,86
+3VS_VGA	74,75,86,87,91
+VGA_VCORE	75,87
+5VS	30,31,36,48,50,51,56,61,80,87,91

20141024 Chris

Remove +3V, +1.35V, +0.675VS, +1.5VS, +1.05VS, +12VS, +VCORE discharge circuit for more space  
20131014

all MOS mount for GPU Optimus function



<Variant Name>

PEGATRON

PEGATRON PROPRIETARY AND CONFIDENTIAL

Size

Custom

Project Name

TRCUG

Date

Friday, November 28, 2014

Sheet

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of

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Rev

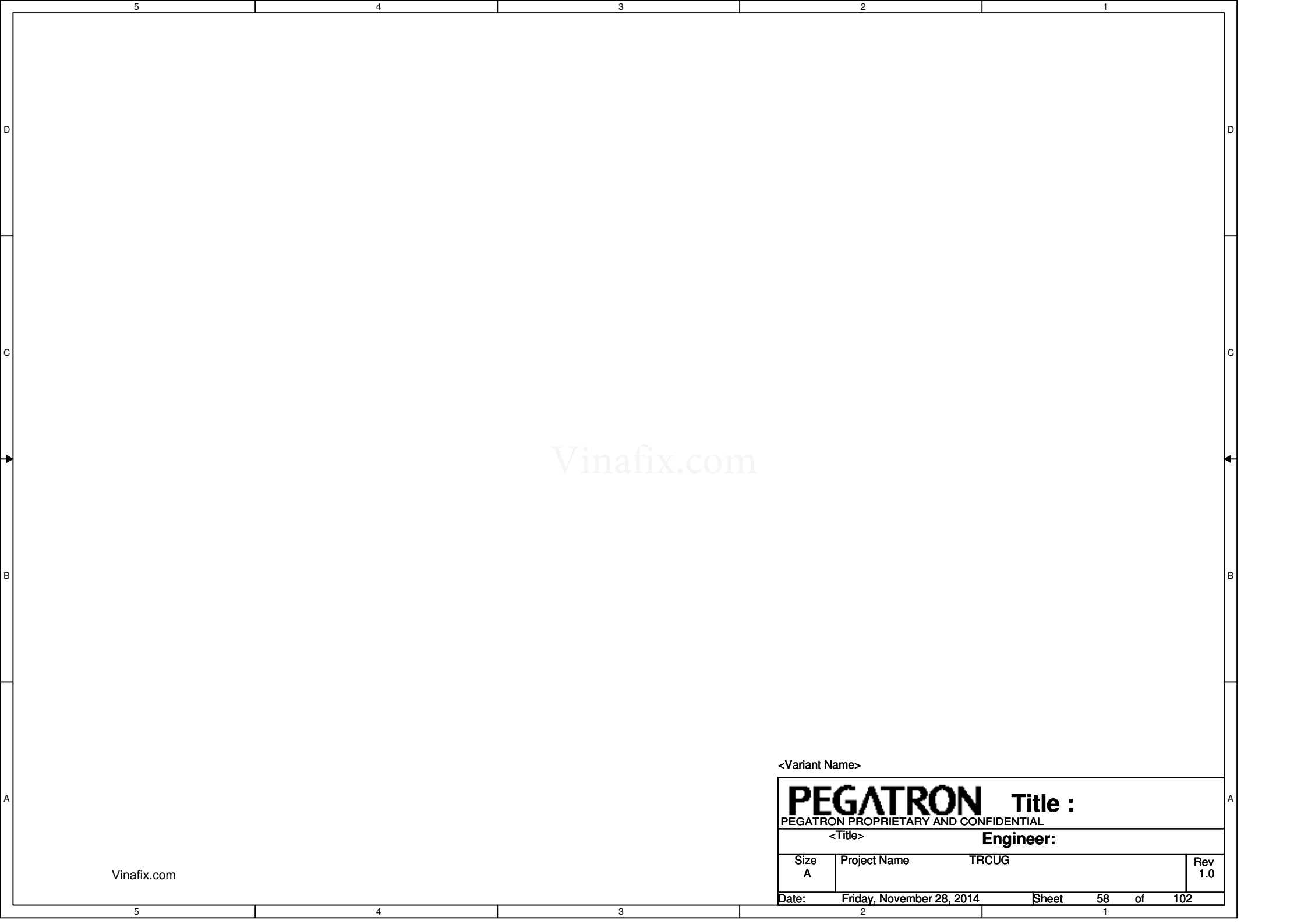
1.0

Title

DSG Discharge

Engineer

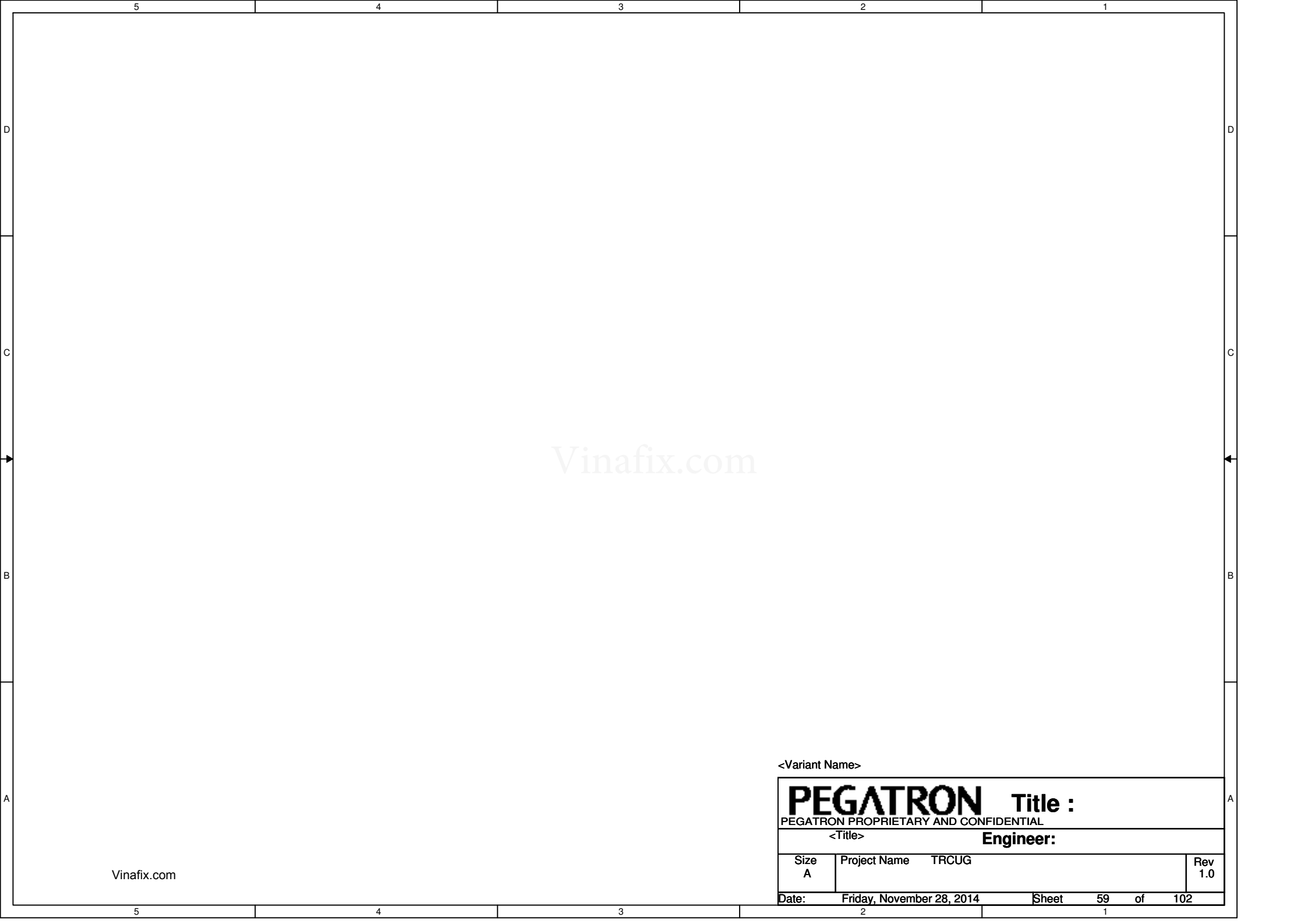
Fenly Chen



Vinafix.com

<Variant Name>

<b>PEGATRON</b> Title :			
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<Title>		Engineer:	
Size A	Project Name TRCUG		Rev 1.0
Date:	Friday, November 28, 2014	Sheet	58 of 102



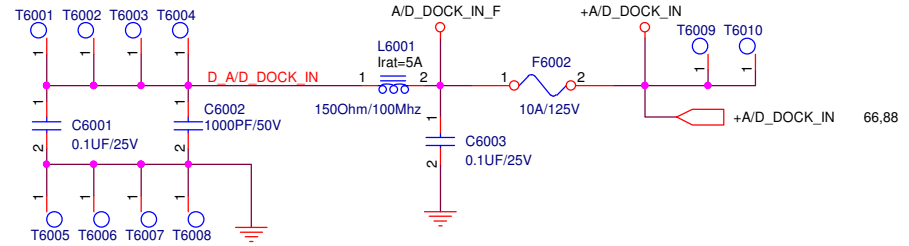
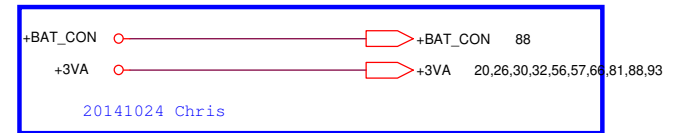
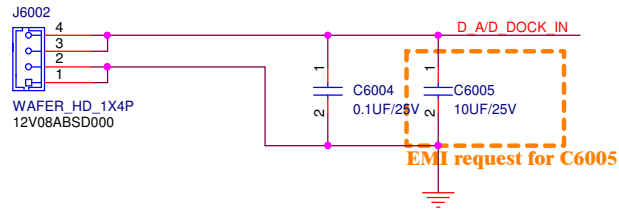
Vinafix.com

Vinafix.com

<Variant Name>

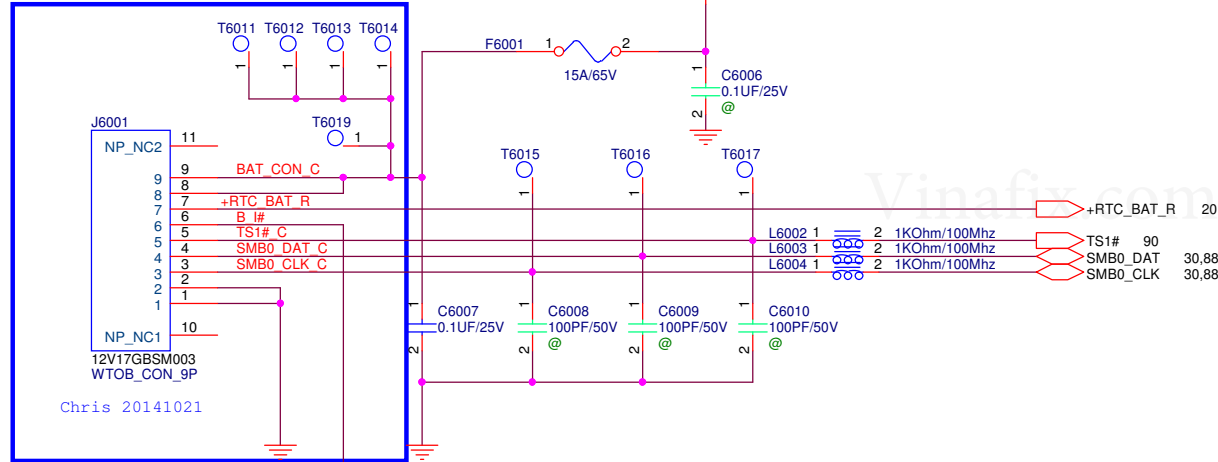
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<Title>		Engineer:	
Size A	Project Name TRCUG		Rev 1.0
Date:	Friday, November 28, 2014	Sheet	59 of 102

## DC IN

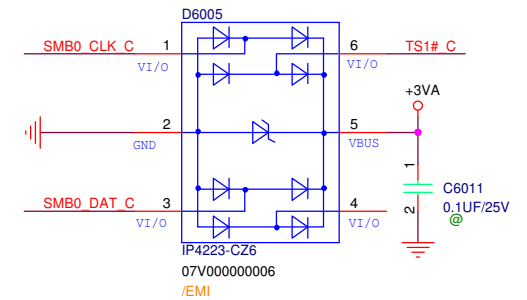


## Battery Connector

Follow MA20 Pin define

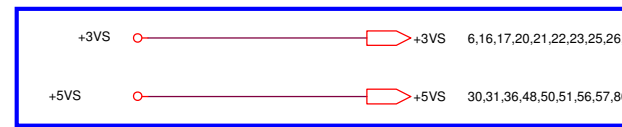


Vinafix.com

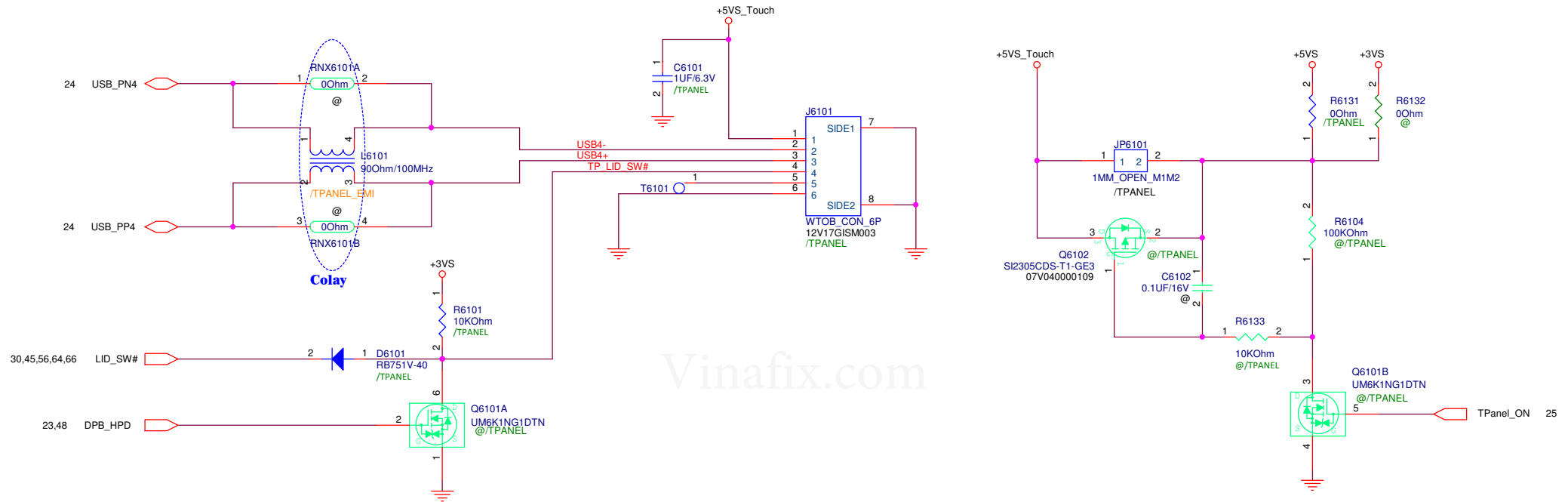


<b>PEGATRON</b>		Title : DC-IN/ DISCHARGE	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
BG1/HW3		Engineer: Fenix Chen	
Size Custom	Project Name <b>TRCUG</b>		Rev 1.0
Date:	Friday, November 28, 2014	Sheet	60 of 102

Vinafix.com

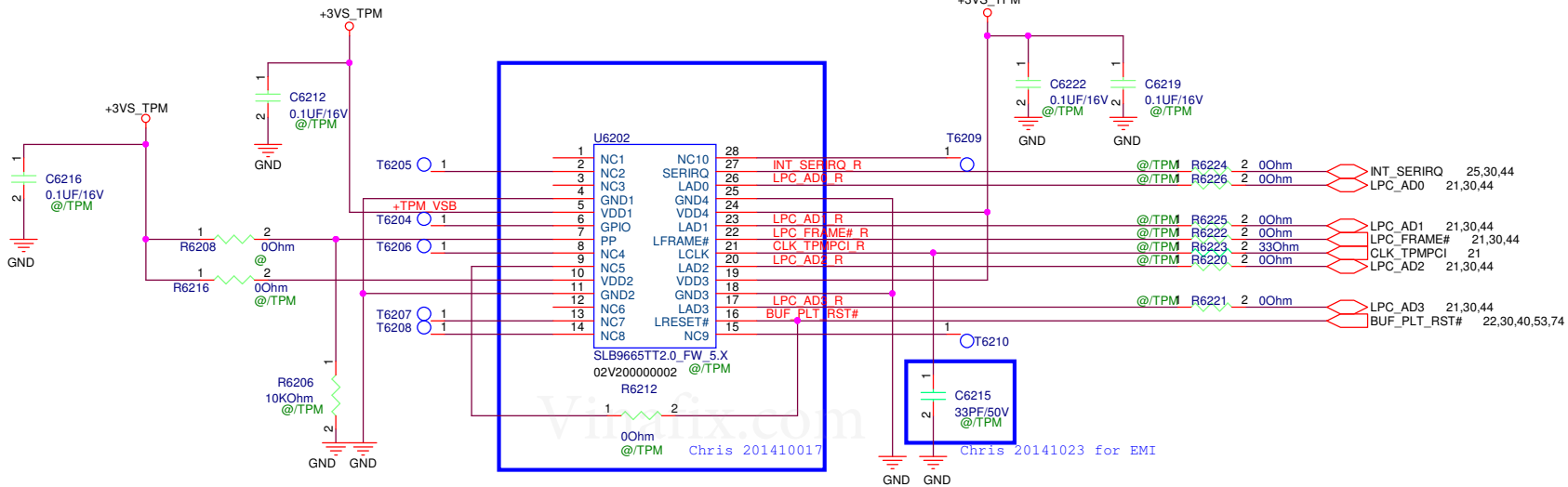
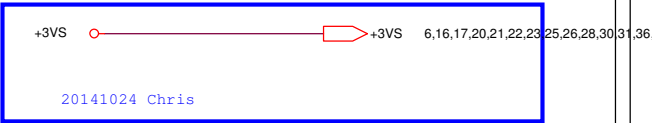
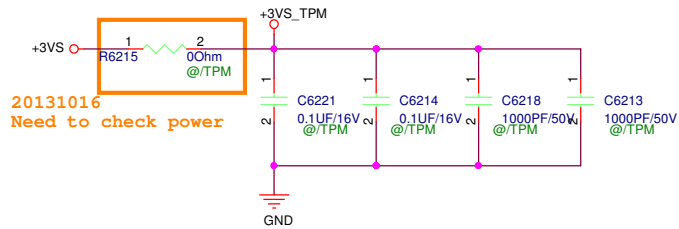


20141024 Chris



<Variant Name>		
<b>PEGATRON</b> Title : Touch Panel Conn		
PEGATRON PROPRIETARY AND CONFIDENTIAL		
BG1/HW3	Engineer: Fenix Chen	
Size Custom	Project Name	Rev 1.0
Date: Friday, November 28, 2014 Sheet 61 of 102		

Infineon TPM 9660 and 9665 Co-lay



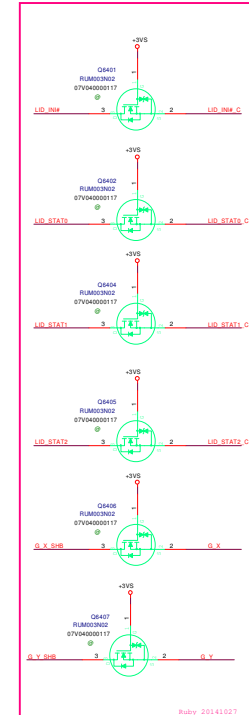
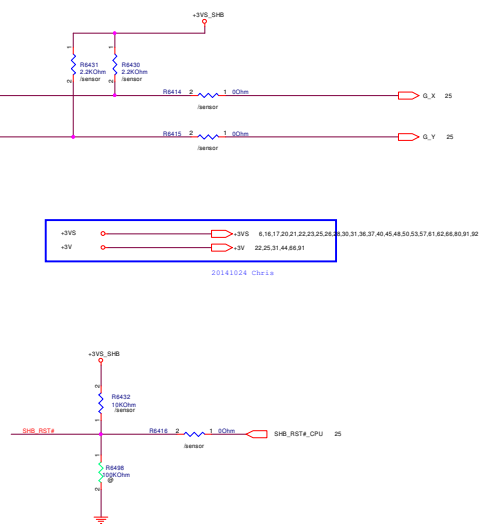
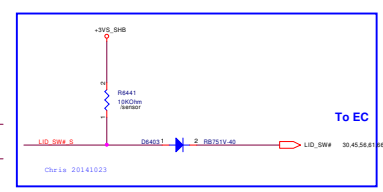
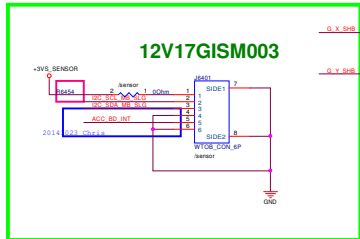
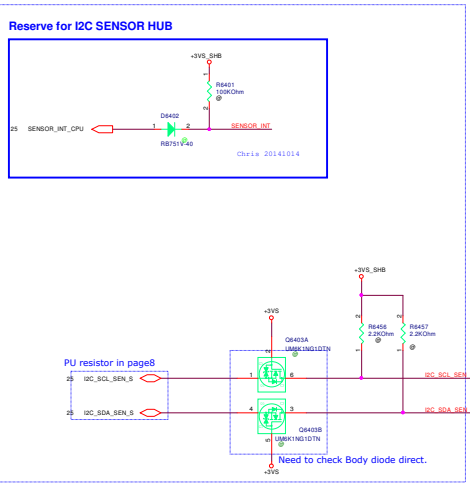
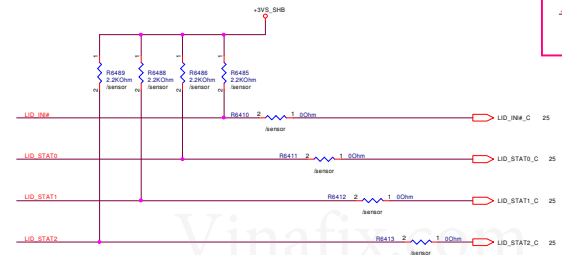
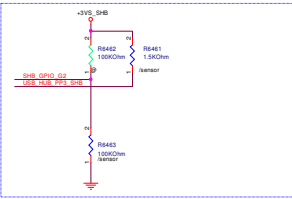
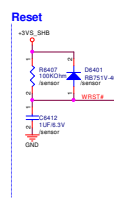
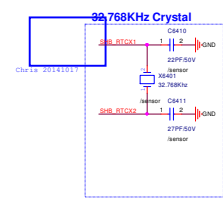
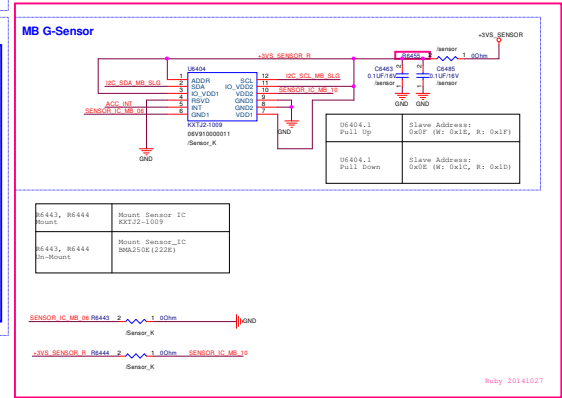
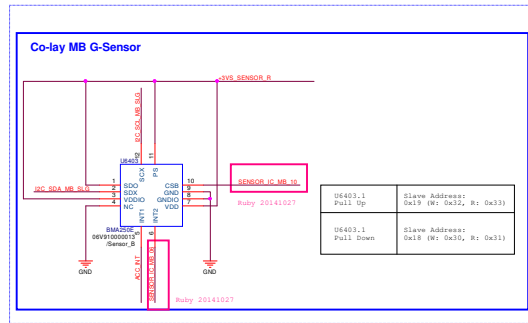
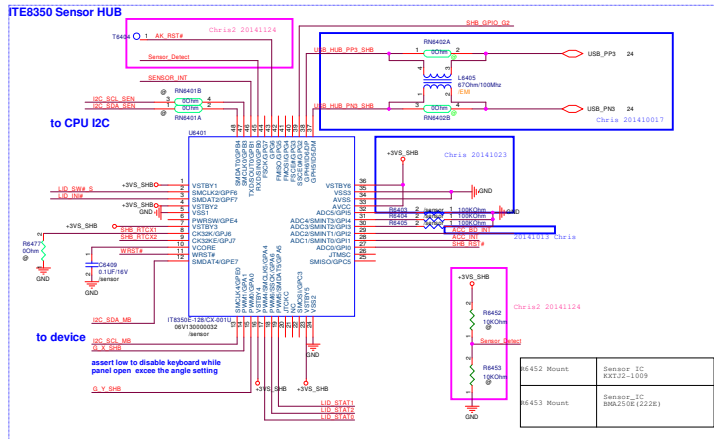
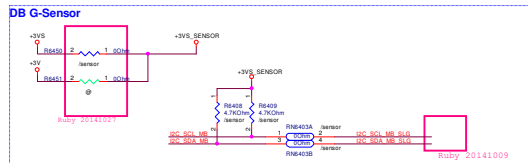
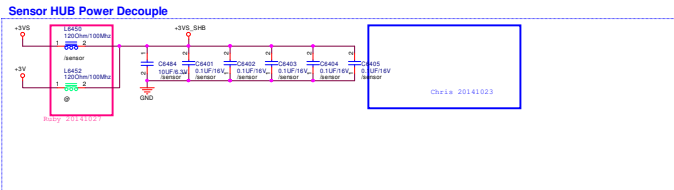
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BG1/HW3		<b>Engineer:</b> <i>Fenix Chen</i>	
Size B	Project Name <b>TRCUG</b>	Rev 1.0	
Date: <u>Friday, November 28, 2014</u>		Sheet	62 of 102

NFC I2C only for Shark Bay platorm

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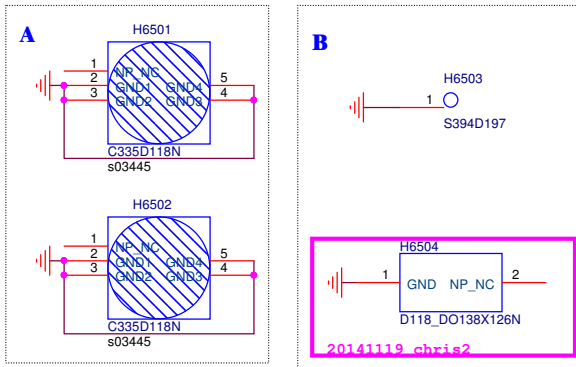
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Size <b>A</b>	Project Name <b>TRCUG</b>		Rev <b>1.0</b>
Date: <b>Friday, November 28, 2014</b>		Sheet <b>63</b> of <b>102</b>	

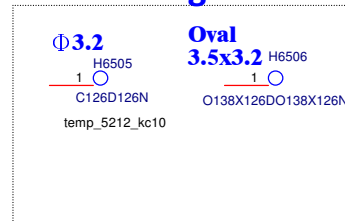




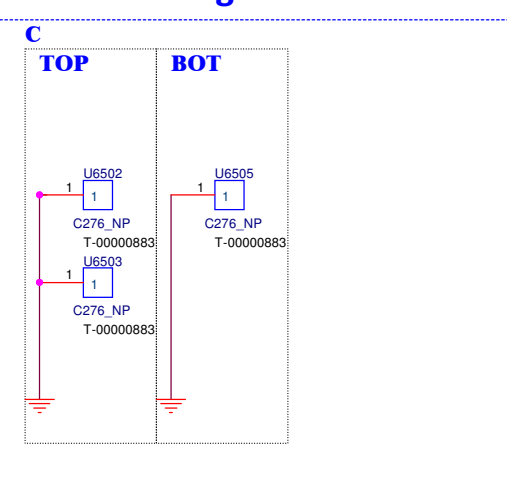
## PCB SCREW HOLE



## PCB Tooling HOLE

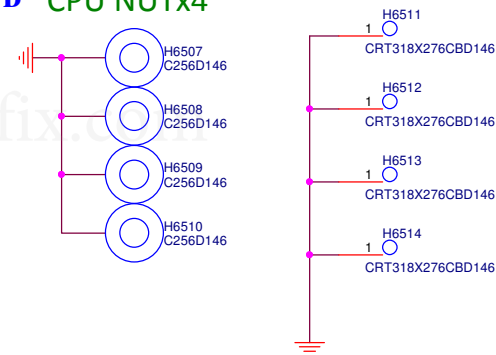


## PCB Sharding PAD



## BGA

### D CPU NUTx4



### VGA NUTx2



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PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Fenix Chen</b>	
Size B	Project Name <b>TRCUG</b>		Rev 1.0
Date: <b>Friday, November 28, 2014</b>		Sheet <b>65</b>	of <b>102</b>



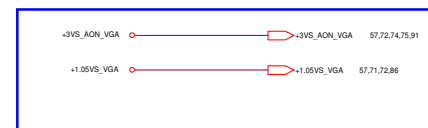
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C					C					
B					B					
A					A					
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Size A	Project Name	TRCUG	Rev 1.0							
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Date:	Friday, November 28, 2014	Sheet	67	of	102					
5	4	3	2	1						

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C					C
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PEGATRON PROPRIETARY AND CONFIDENTIAL		
<Title> Engineer:		
Size A	Project Name TRCUG	Rev 1.0
Date:	Friday, November 28, 2014	Sheet 68 of 102

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Size A	Project Name	TRCUG	Rev 1.0					
<div>Date: Friday, November 28, 2014</div>								
<div>Sheet 69 of 102</div>								



```
For cost down!! SR Check!!
unmount:U7002, R7009
mount: D7001,R7005
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&lt;Variant Name

REGISTRATION PROPRIETARY AND CONFIDENTIAL			
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Size Custom	Project Name TRCUG		Rev. 1.
Date:	Friday, November 26, 2014	Sheet	70 of 103

76.77 FBAD[0..63]  
76.77 FBA\_CMD[0..30]  
76.77 FBADQM[0..7]  
76.77 FBADQS\_WP[0..7]  
76.77 FBADQS\_RN[0..7]

U7001B  
2/14 FBA

FBA00	E18	FBA_D0
FBA01	F18	FBA_D1
FBA02	E16	FBA_D2
FBA03	F17	FBA_D3
FBA04	D20	FBA_D4
FBA05	D21	FBA_D5
FBA06	F20	FBA_D6
FBA07	E21	FBA_D7
FBA08	E15	FBA_D8
FBA09	D15	FBA_D9
FBA10	F15	FBA_D10
FBA11	F13	FBA_D11
FBA12	C13	FBA_D12
FBA13	B13	FBA_D13
FBA14	E13	FBA_D14
FBA15	D13	FBA_D15
FBA16	B15	FBA_D16
FBA17	C16	FBA_D17
FBA18	A13	FBA_D18
FBA19	A15	FBA_D19
FBA20	B16	FBA_D20
FBA21	A18	FBA_D21
FBA22	A19	FBA_D22
FBA23	C19	FBA_D23
FBA24	B24	FBA_D24
FBA25	C23	FBA_D25
FBA26	A25	FBA_D26
FBA27	A24	FBA_D27
FBA28	A21	FBA_D28
FBA29	B21	FBA_D29
FBA30	C20	FBA_D30
FBA31	C21	FBA_D31
FBA32	F22	FBA_D32
FBA33	F24	FBA_D33
FBA34	T22	FBA_D34
FBA35	R24	FBA_D35
FBA36	N25	FBA_D36
FBA37	N26	FBA_D37
FBA38	N23	FBA_D38
FBA39	N24	FBA_D39
FBA40	V23	FBA_D40
FBA41	V22	FBA_D41
FBA42	T23	FBA_D42
FBA43	U22	FBA_D43
FBA44	Y24	FBA_D44
FBA45	AA24	FBA_D45
FBA46	Y22	FBA_D46
FBA47	AA23	FBA_D47
FBA48	AD27	FBA_D48
FBA49	AB26	FBA_D49
FBA50	AD26	FBA_D50
FBA51	AC25	FBA_D51
FBA52	AA27	FBA_D52
FBA53	AA26	FBA_D53
FBA54	W26	FBA_D54
FBA55	Y25	FBA_D55
FBA56	R26	FBA_D56
FBA57	T25	FBA_D57
FBA58	N27	FBA_D58
FBA59	R27	FBA_D59
FBA60	V26	FBA_D60
FBA61	V27	FBA_D61
FBA62	W27	FBA_D62
FBA63	W25	FBA_D63

FBA0QM0	D19	FBA_DQM0
FBA0QM1	D14	FBA_DQM1
FBA0QM2	C17	FBA_DQM2
FBA0QM3	C22	FBA_DQM3
FBA0QM4	P24	FBA_DQM4
FBA0QM5	W24	FBA_DQM5
FBA0QM6	AA25	FBA_DQM6
FBA0QM7	U25	FBA_DQM7

FBA0QS_WP0	E19	FBA_DQS_WP0
FBA0QS_WP1	C15	FBA_DQS_WP1
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FBA0QS_WP4	R25	FBA_DQS_WP4
FBA0QS_WP5	W23	FBA_DQS_WP5
FBA0QS_WP6	AB26	FBA_DQS_WP6
FBA0QS_WP7	T26	FBA_DQS_WP7

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FBA0QS_RN3	A22	FBA_DQS_RN3
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FBA0QS_RN5	W22	FBA_DQS_RN5
FBA0QS_RN6	AB27	FBA_DQS_RN6
FBA0QS_RN7	T27	FBA_DQS_RN7

NC	FB_CLAMP
GF119	GF117/GK208

35 mA

FBA_CMD34	FBA_CMD34
FBA_CMD35	FBA_CMD35

FB_PLLAVDD	FB_PLL_AVDD_1
FB_PLLAVDD	FB_PLL_AVDD_2
FB_DLLAVDD	FB_DLL_AVDD
GF117	GF119/GK208

T7101  
1 FB\_VREF  
D23  
FB\_VREF  
N155-GT-S-A2  
02V0A0000032  
/VGA

GPU\_FB\_CLAMP\_R R7107 2 1 00Ohm  
GC6\_FB\_EN 25,74,91

R7106 2  
/VGA  
1 10KOhm  
1%

FBA\_CMD0  
C27  
FBA\_CMD1  
C26  
FBA\_CMD2  
C24  
FBA\_CMD3  
C23  
FBA\_CMD4  
C22  
FBA\_CMD5  
C21  
FBA\_CMD6  
C20  
FBA\_CMD7  
C19  
FBA\_CMD8  
C18  
FBA\_CMD9  
C17  
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C13  
FBA\_CMD27  
C12  
FBA\_CMD28  
C11  
FBA\_CMD29  
C10  
FBA\_CMD30  
C09  
FBA\_CMD31  
C08

FBA\_ODT\_L FBA\_CMD2 R7103 2 /VGA 1 10KOhm  
FBA\_ODT\_H FBA\_CMD18 R7104 2 /VGA 1 10KOhm  
FBA\_CKE\_L FBA\_CMD3 R7154 2 /VGA 1 10KOhm  
FBA\_CKE\_H FBA\_CMD19 R7108 2 /VGA 1 10KOhm

+1.35VS\_VGA  
F22 R7101 1 2 60.4Ohm 1%  
J22 R7102 1 2 60.4Ohm 1%

D24 FBA\_CLK0 76  
D25 FBA\_CLK0# 76  
N22 FBA\_CLK1 77  
M22 FBA\_CLK1# 77

FBA\_WCK01 D18  
FBA\_WCK01\_N C18  
FBA\_WCK02 D17  
FBA\_WCK02\_N D16  
FBA\_WCK23\_N T24  
FBA\_WCK45 U24  
FBA\_WCK45\_N V24  
FBA\_WCK67 V25

1.05V+3% 100 mA  
C7118 10UF/10V /VGA 10%  
C7104 10UF/10V /VGA 10%  
C7101 300nF/100Mhz /VGA 10%  
C7103 22UF/6.3V /VGA 10%  
B7101 2 000  
09V0100000029  
Place NEAR GPU

+1.35VS\_VGA  
+1.05VS\_VGA  
57,75,76,77,91  
57,70,72,86

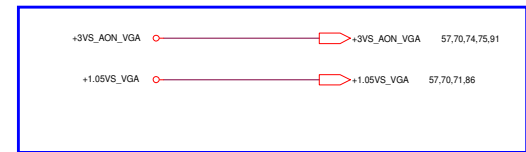
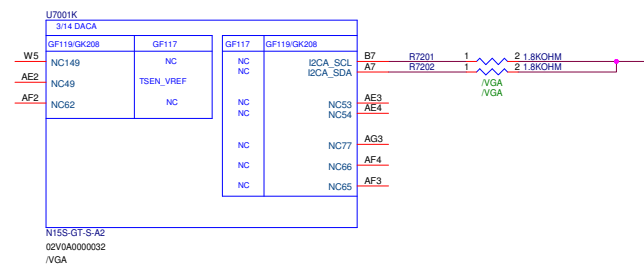
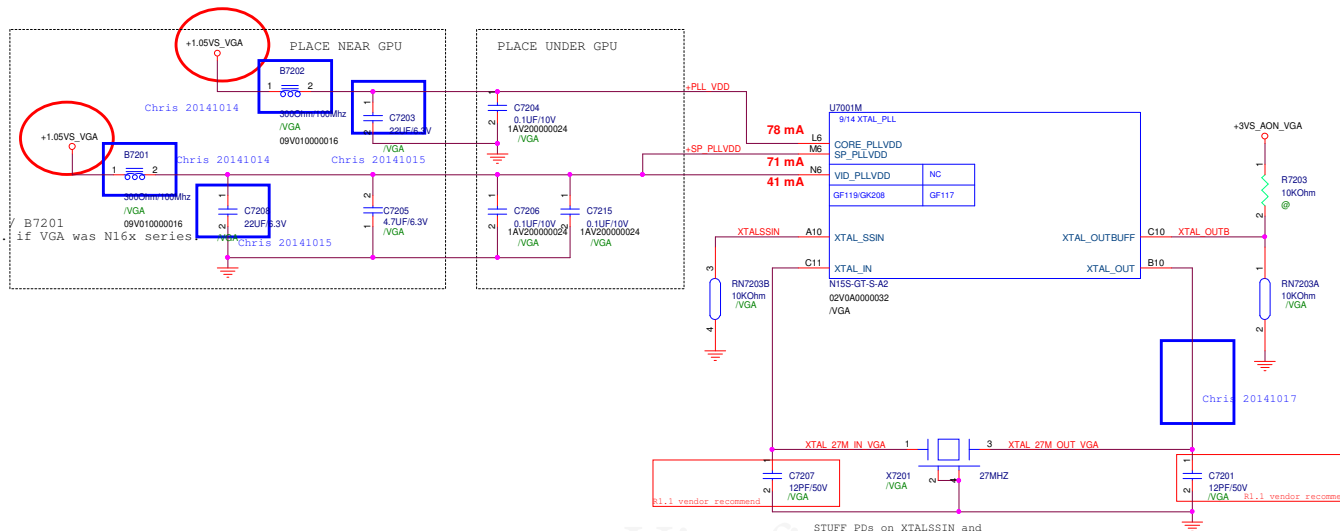
GC6\_RST  
FBA\_CMD5  
VRAM\_RST# 76,77  
R7153 10KOhm  
/VGA  
1%  
1

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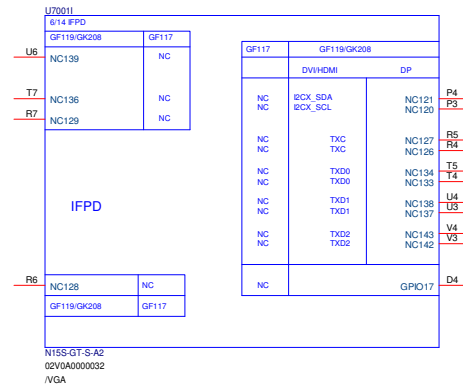
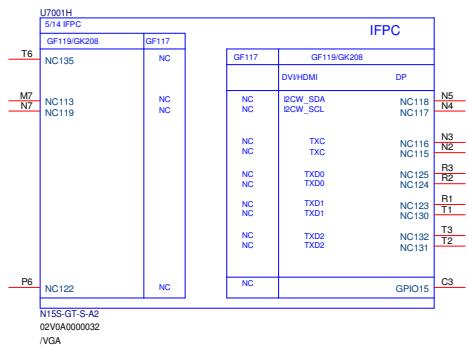
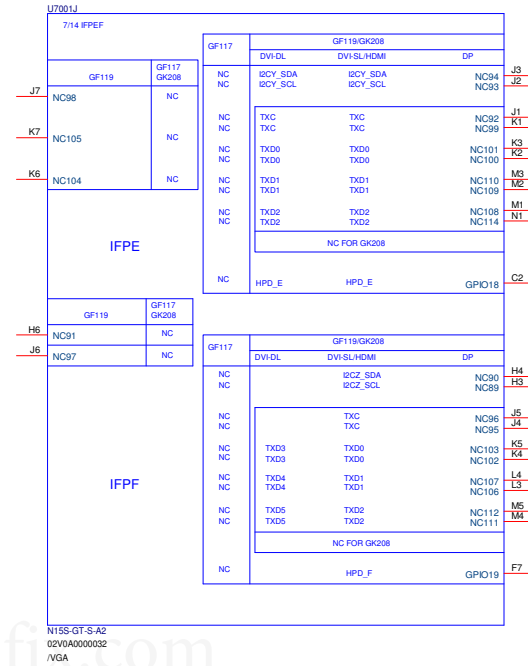
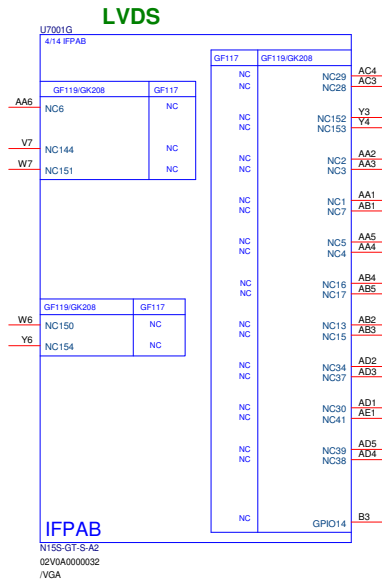
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Engineer:  
Size C Project Name TRCUG Rev 1.0  
Date: Friday, November 28, 2014 Sheet 71 of 103

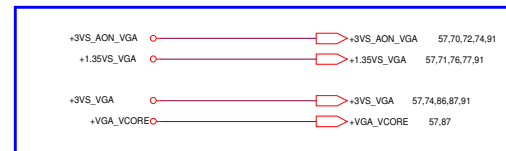
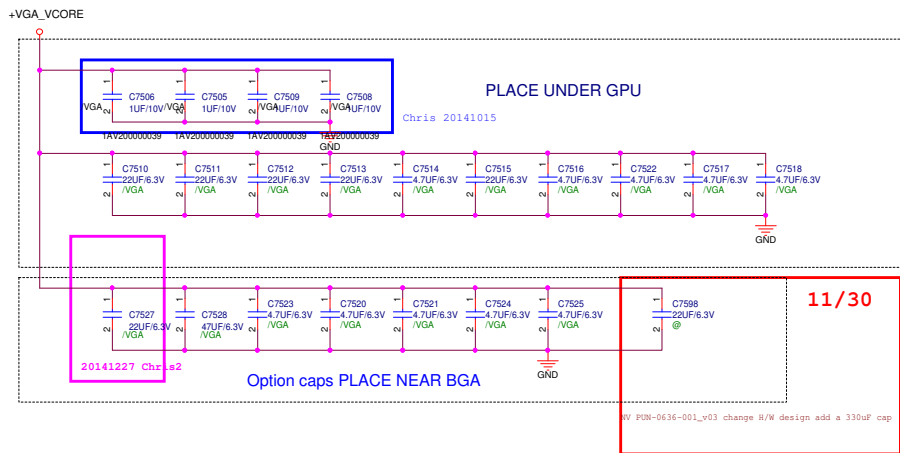
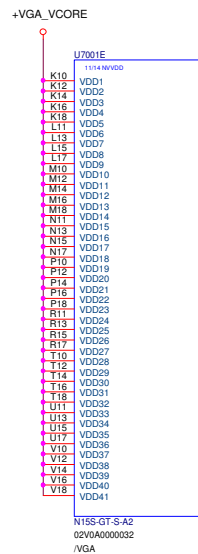
07.06 FAE recommend B7202 need change to 300ohm bead, if VGA was N16x series



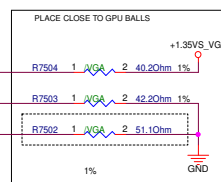
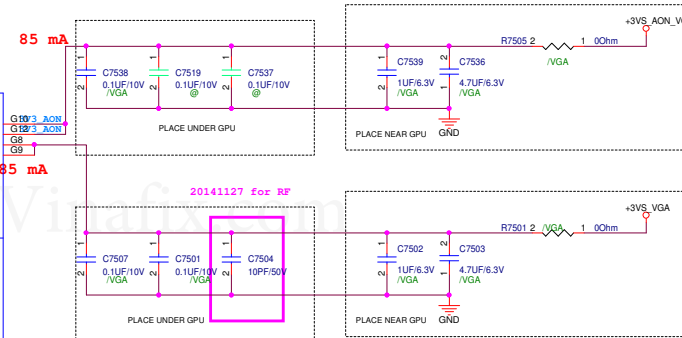
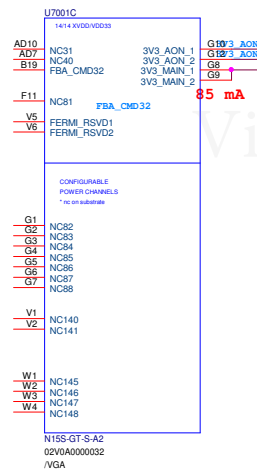
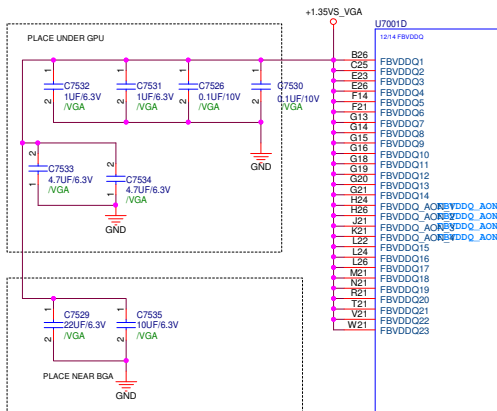
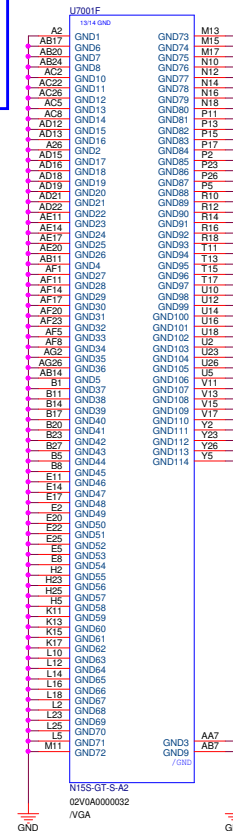








20141024 Chris



<Variant Name>

**PEGATRON** Title :

PEGATRON PROPRIETARY AND CONFIDENTIAL

<Title> Engineer:

Size	Project Name	TRCUG	Rev
C			1.0

Date: Friday, November 28, 2014 Sheet 75 of 103

# FBA Partition 31..0 RANK 0

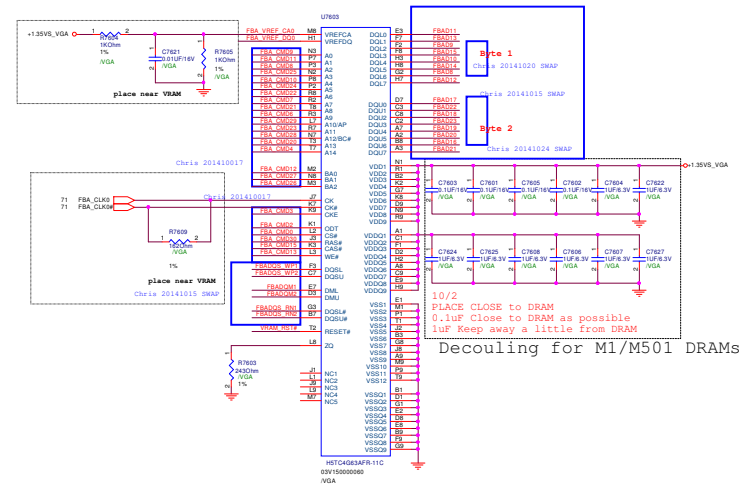
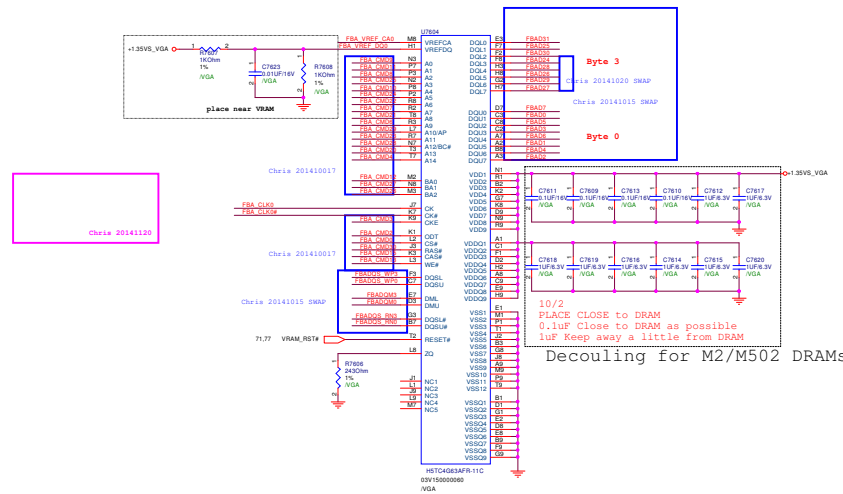
71.77 FBA00L031  
71.77 FBA00L032  
71.77 FBA00L033  
71.77 FBA00L034

+1.35V\_VGA -> +1.35V\_VGA 57.71.75.77.81

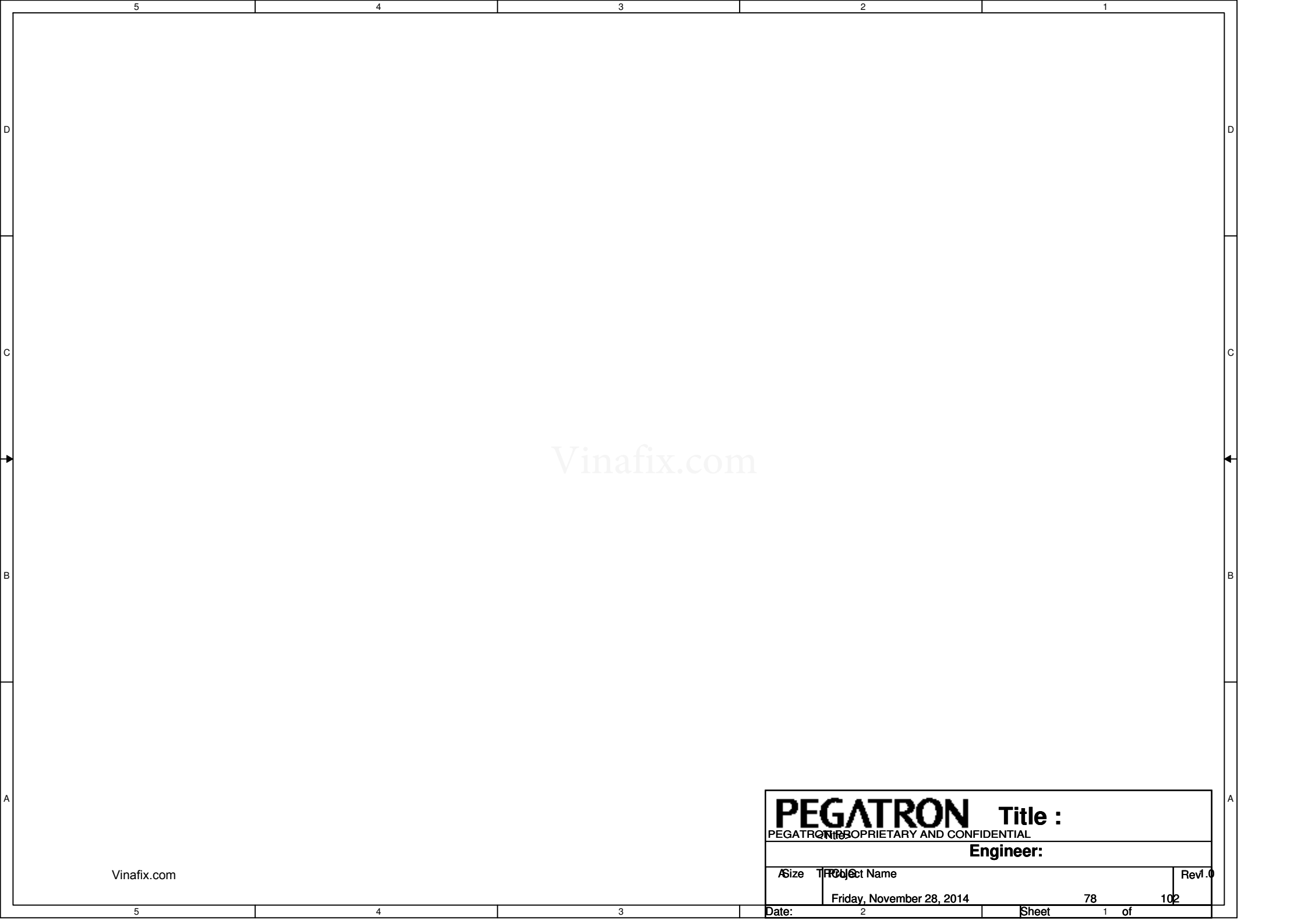
20141004 Chris

\*TOP SIDE\* --- M2

\*BOT SIDE\* --- M0

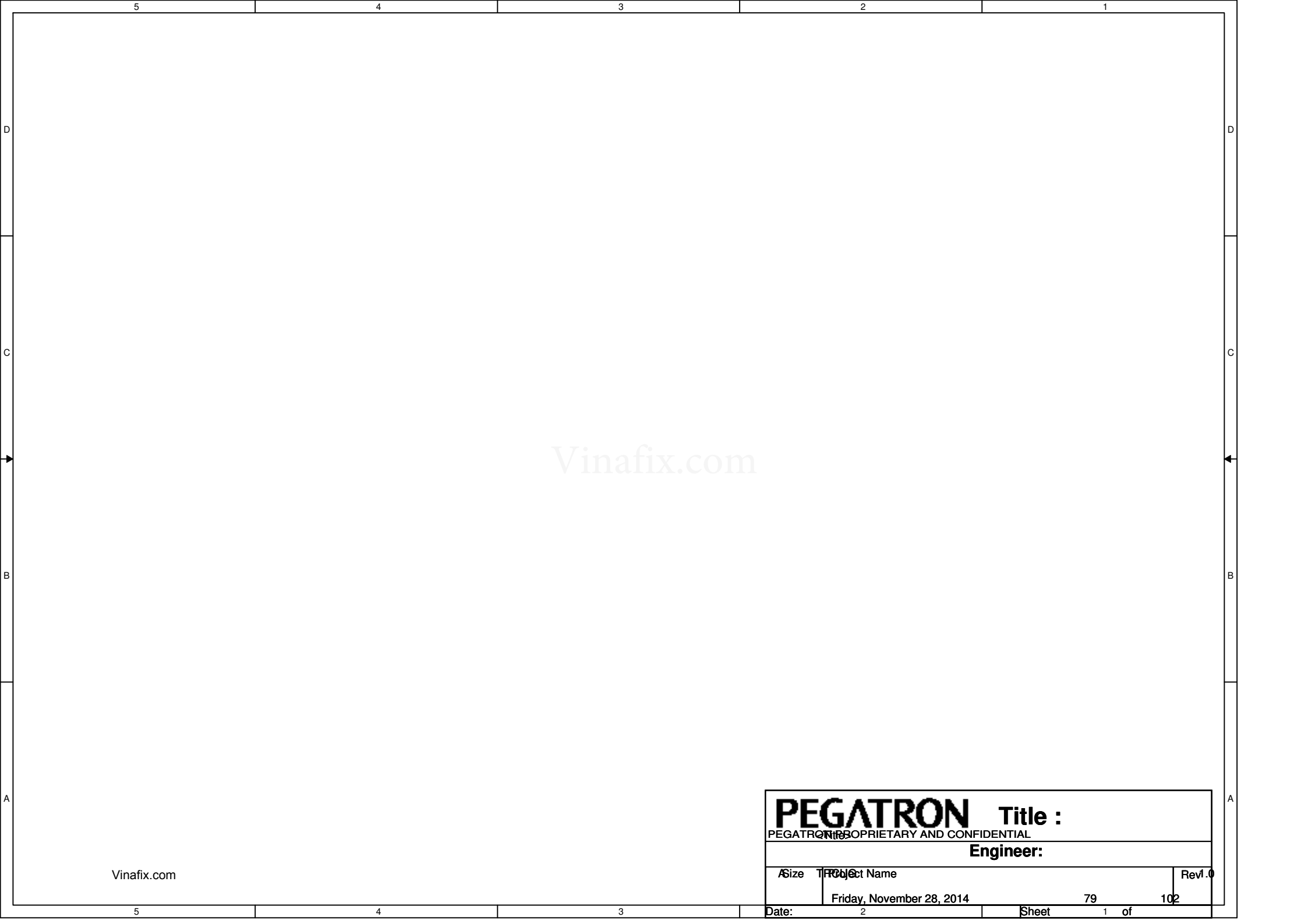






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PEGATRON PROPRIETARY AND CONFIDENTIAL			
<b>Engineer:</b>			
Size	Project Name	Rev	
	Friday, November 28, 2014	78	102
Date:		Sheet	1 of 1



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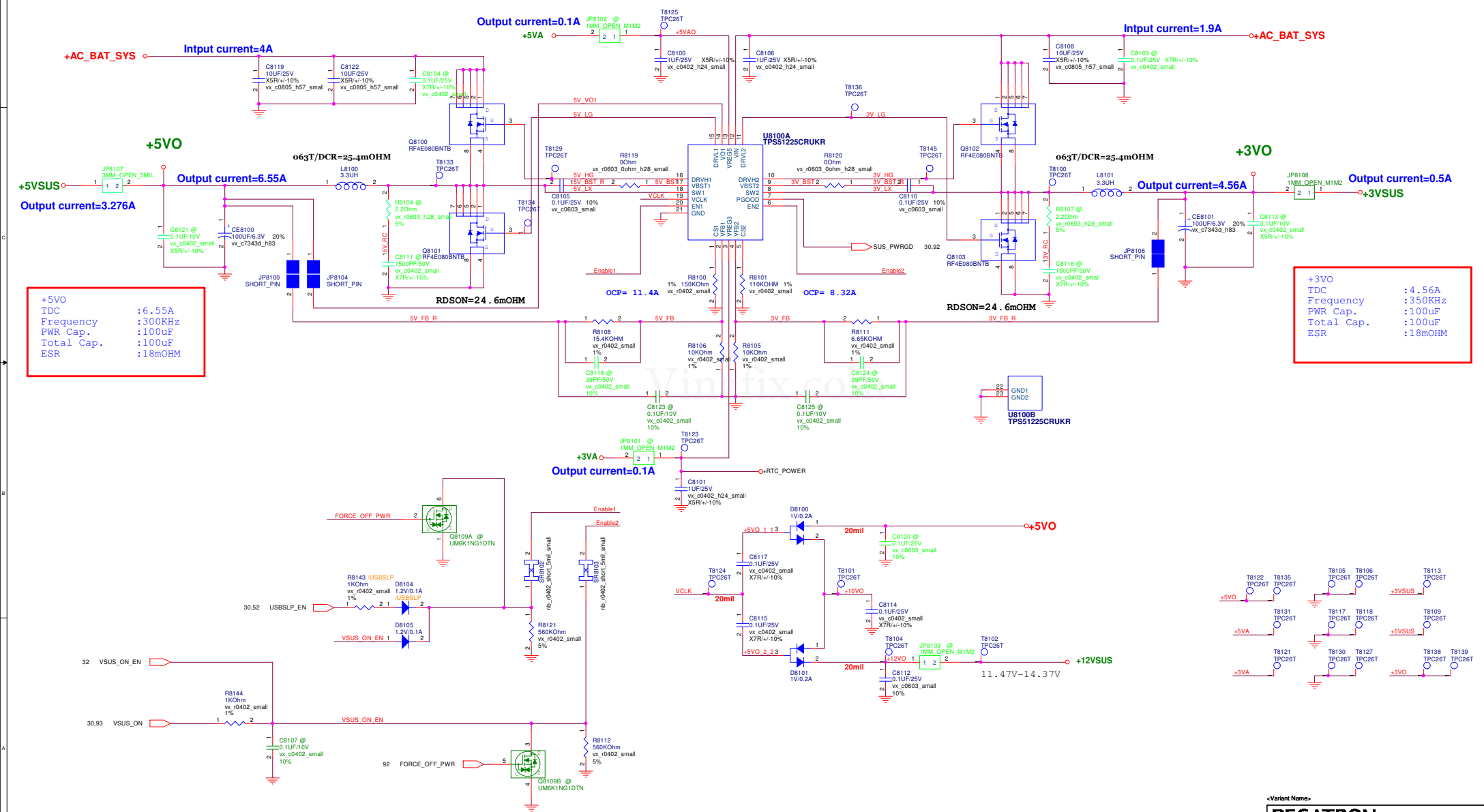
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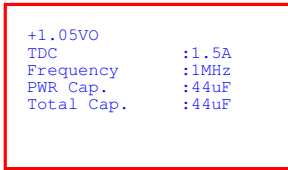
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Size	Project Name	Rev1.0	
	Friday, November 28, 2014	79	102
Date:	2	Sheet	1 of



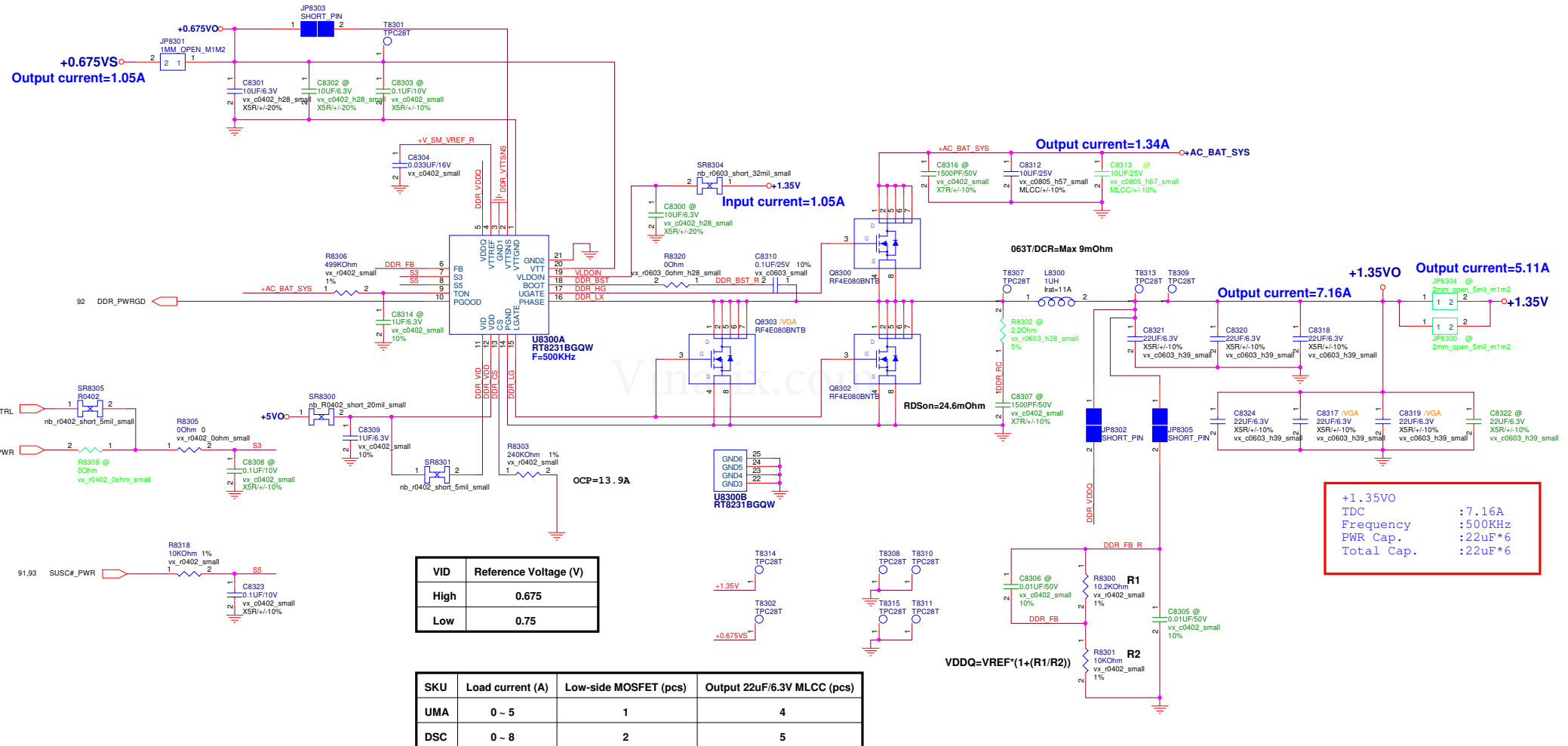


## +5VO & +3VO POWER SUPPLY

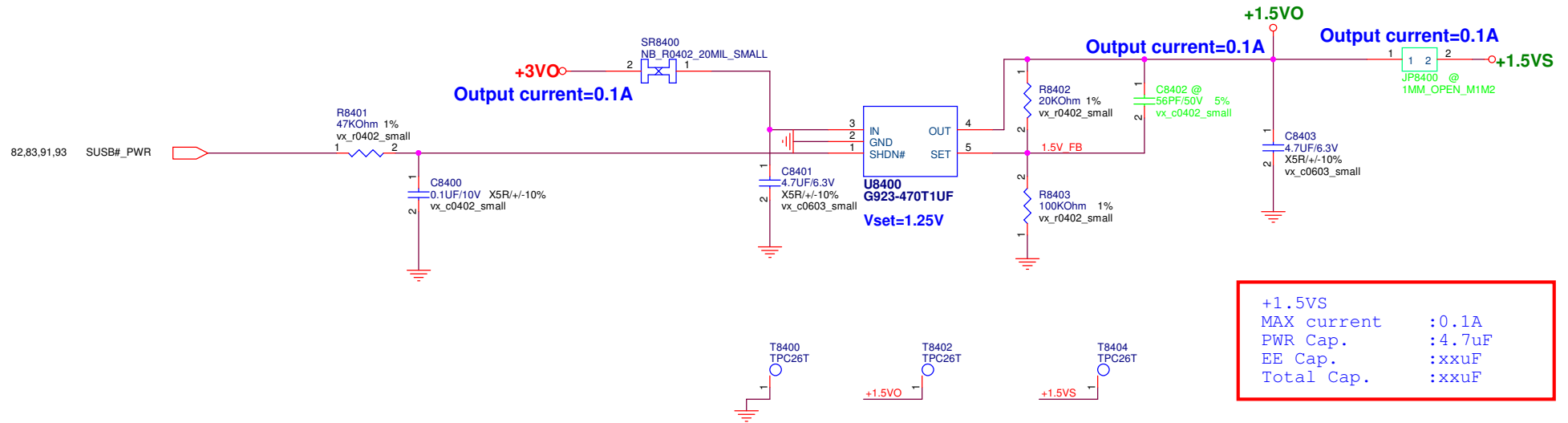





## DDR & VTT POWER SUPPLY



## 1.5VS POWER SUPPLY



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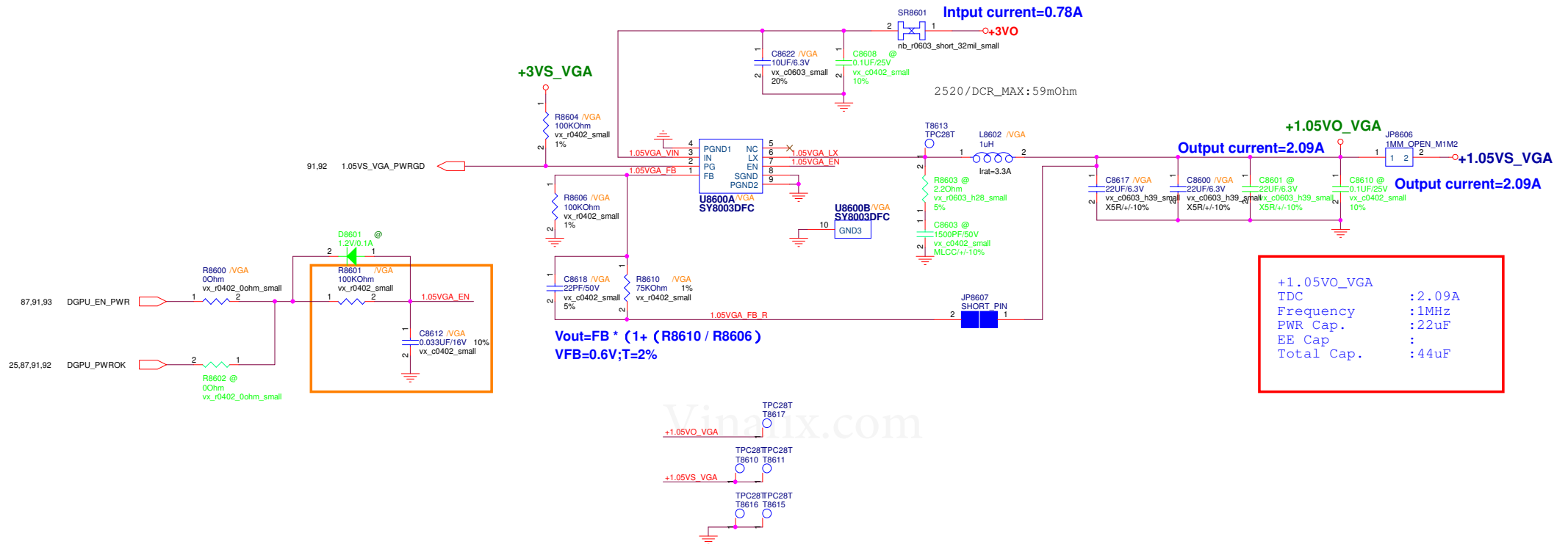
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer:</b> Neil Lin	
Size B	Project Name AR10CU		Rev 1.0
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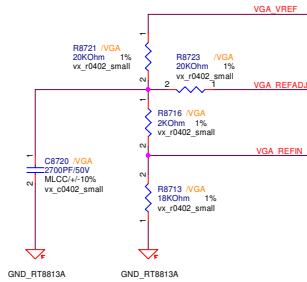
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Size <b>C</b>	Project Name <b>TRCUG</b>	Rev <b>1.0</b>	
Date: <b>Friday, November 28, 2014</b>		Sheet	<b>85</b> of <b>103</b>

## +1.05VS\_VGA POWER SUPPLY



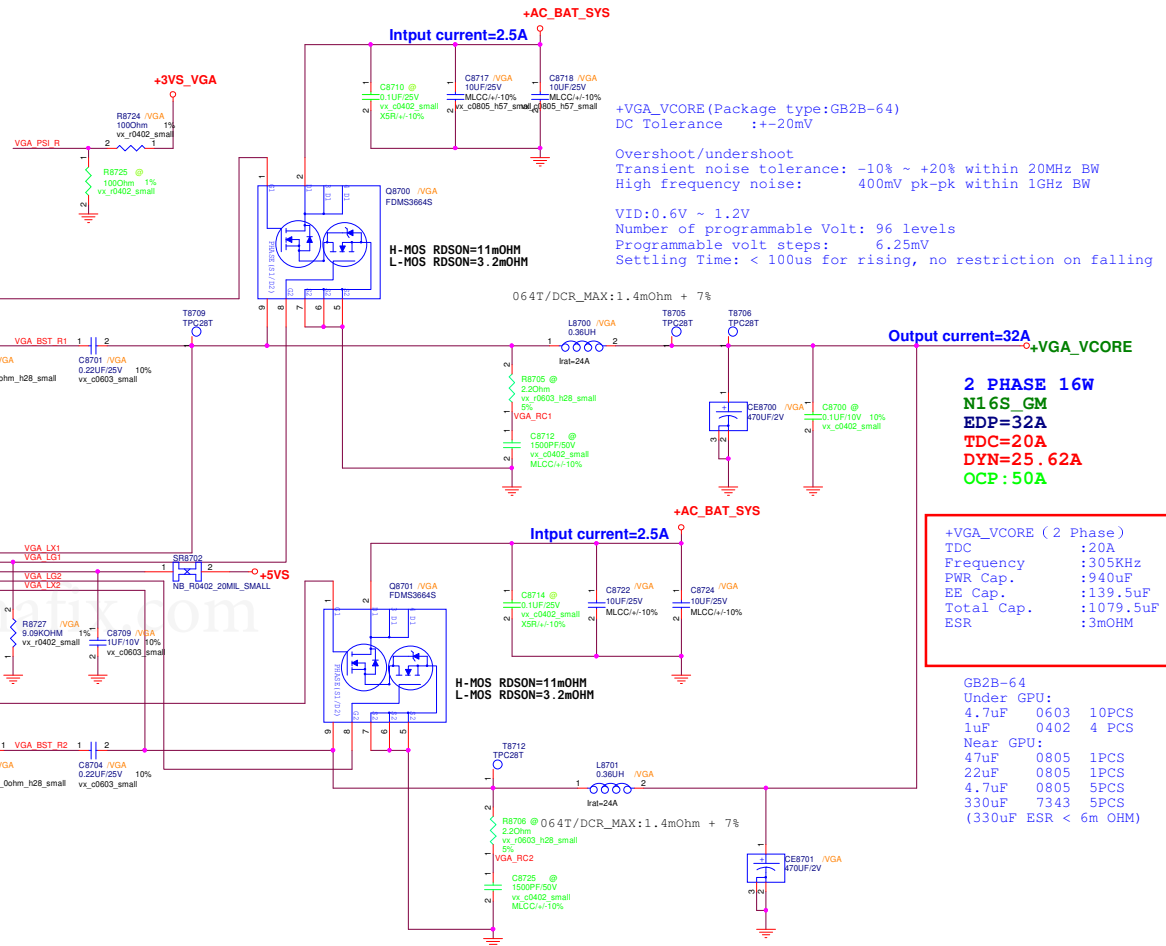
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer:	<b>Neil Lin</b>
Size Custom	Project Name	<b>TRCUG</b>	Rev 1.0
Date:	<b>Friday, November 28, 2014</b>	Sheet	<b>86 of 103</b>

# VGA\_CORE POWER SUPPLY



	N16	N16S_GM
R8723	39K	20K
R8721	39K	20K
R8716	1.5K	2K
R8713	31.5K	18K
C8720	>1.8nF	2.7nF
Vstep	6.25mV	6.25mV
Vmin	0.65V	0.6V
Vmax	1.15V	1.2V
Vboot	0.875V	0.9V
openVr Config	A	B

VGA_PSI#	VO_action
~ 0.8V	1 Phase DEM
1.2 ~ 1.8V	1 Phase FCCM
2.4V ~	2 Phase FCCM

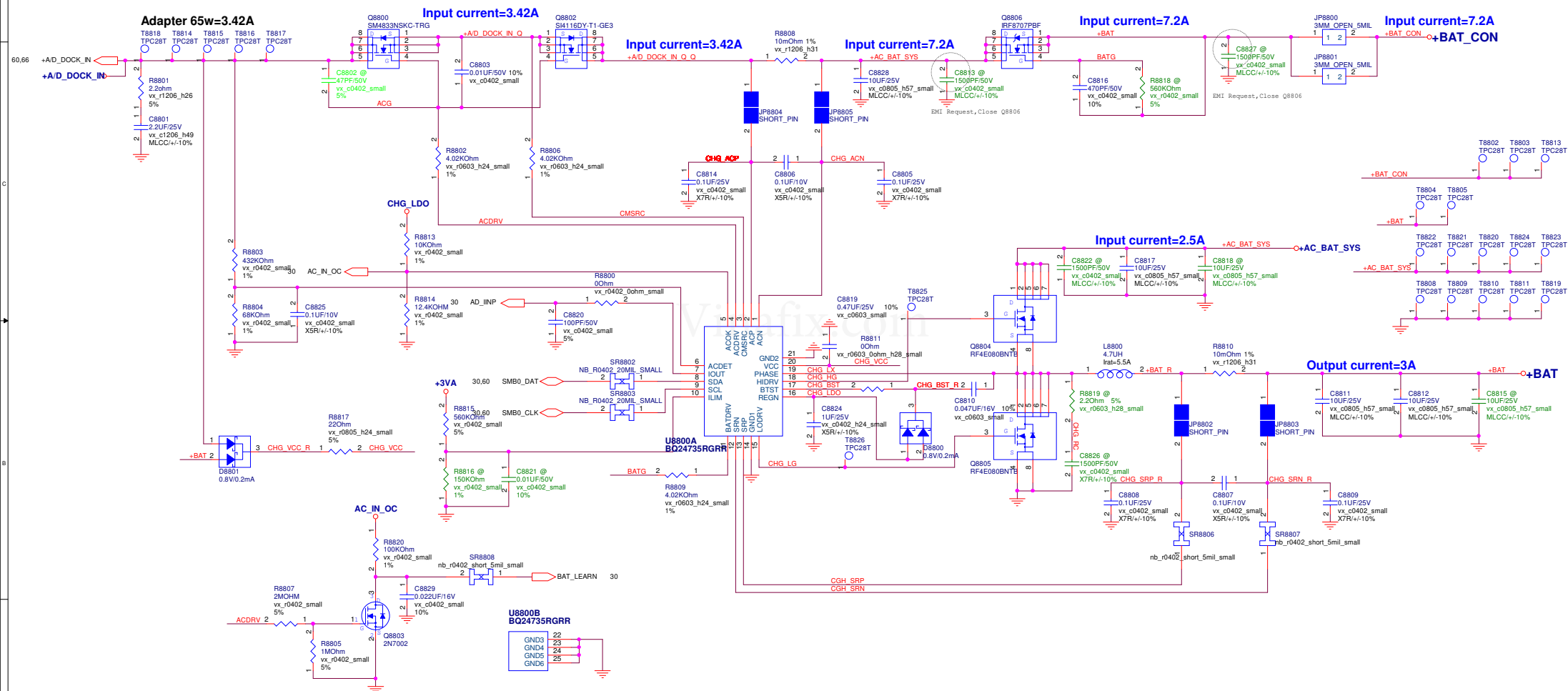


EE side pull high OHM check

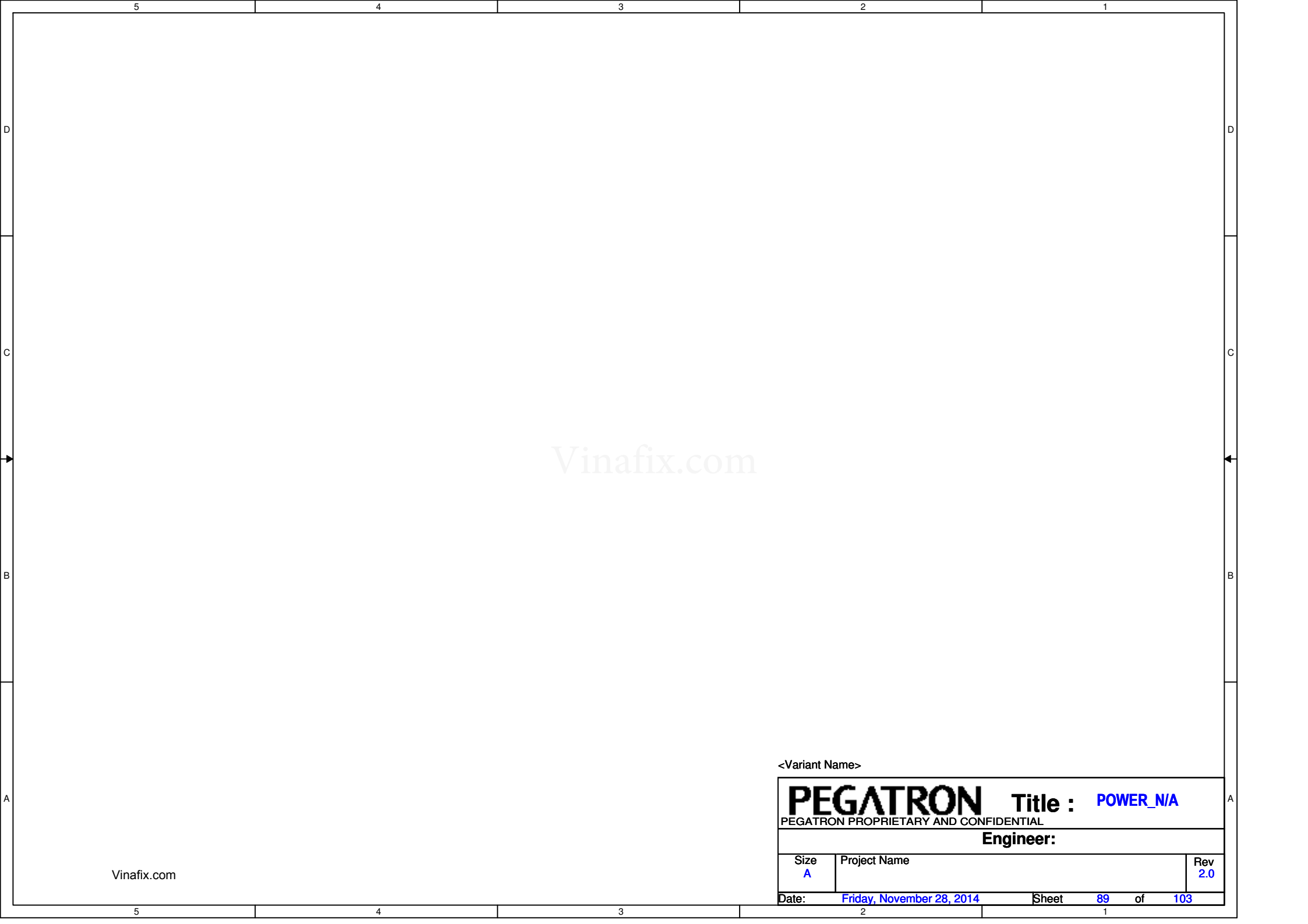
<Variant Name>

PEGATRON		Title	POWER_VGA_VCORE
PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer:		Neil Lin	
Size	Project Name	Rev	1.0
Custom	TRCUG		
Date:	Friday, November 28, 2014	Sheet	67 of 80

## BATTERY CHARGER







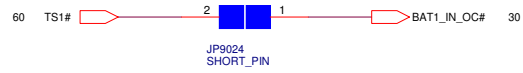
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<Variant Name>

<b>PEGATRON</b>			<b>Title :</b> POWER_N/A		
PEGATRON PROPRIETARY AND CONFIDENTIAL					
<b>Engineer:</b>					
Size A	Project Name				Rev 2.0
Date:	Friday, November 28, 2014		Sheet	89	of 103

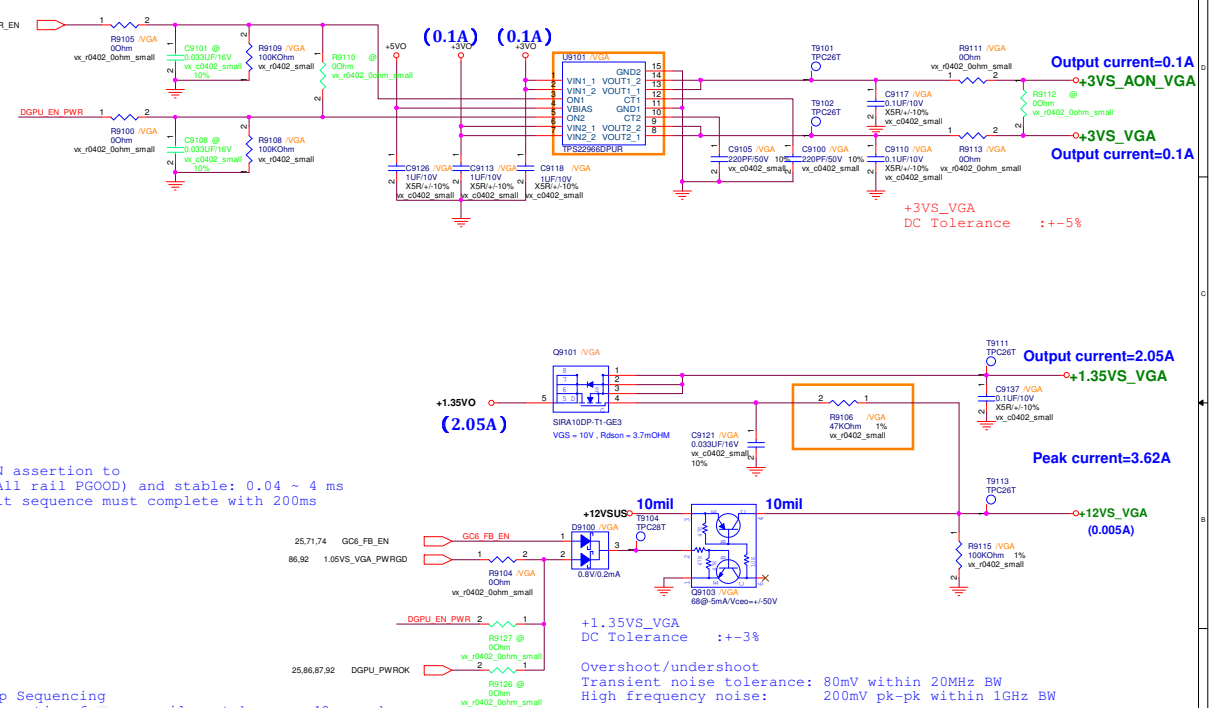
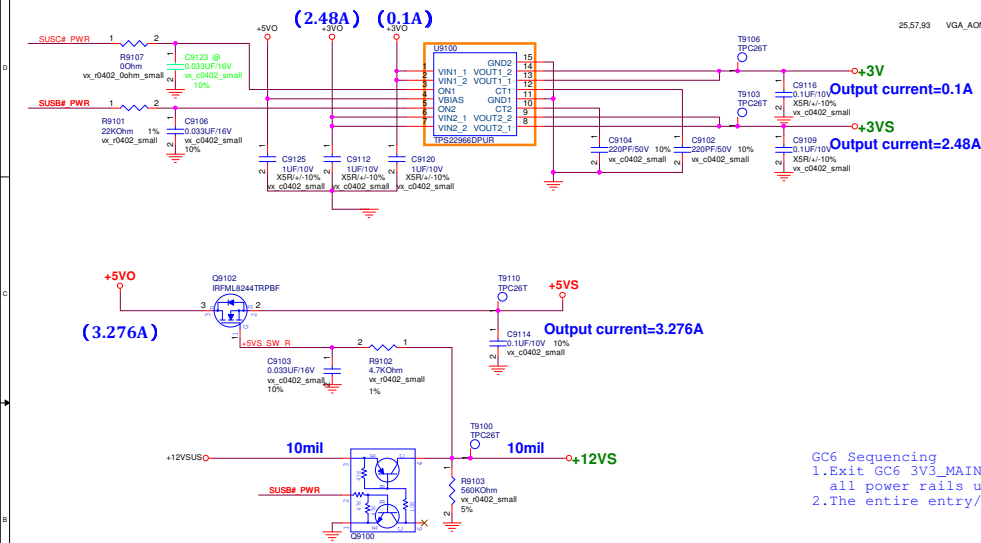
**BATTERY IN DETECT**



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## SUSC#\_PWR and SUBS#\_PWR POWER

## DSC\_VGA\_PWR POWER



### SUSB#\_PWR POWER Control

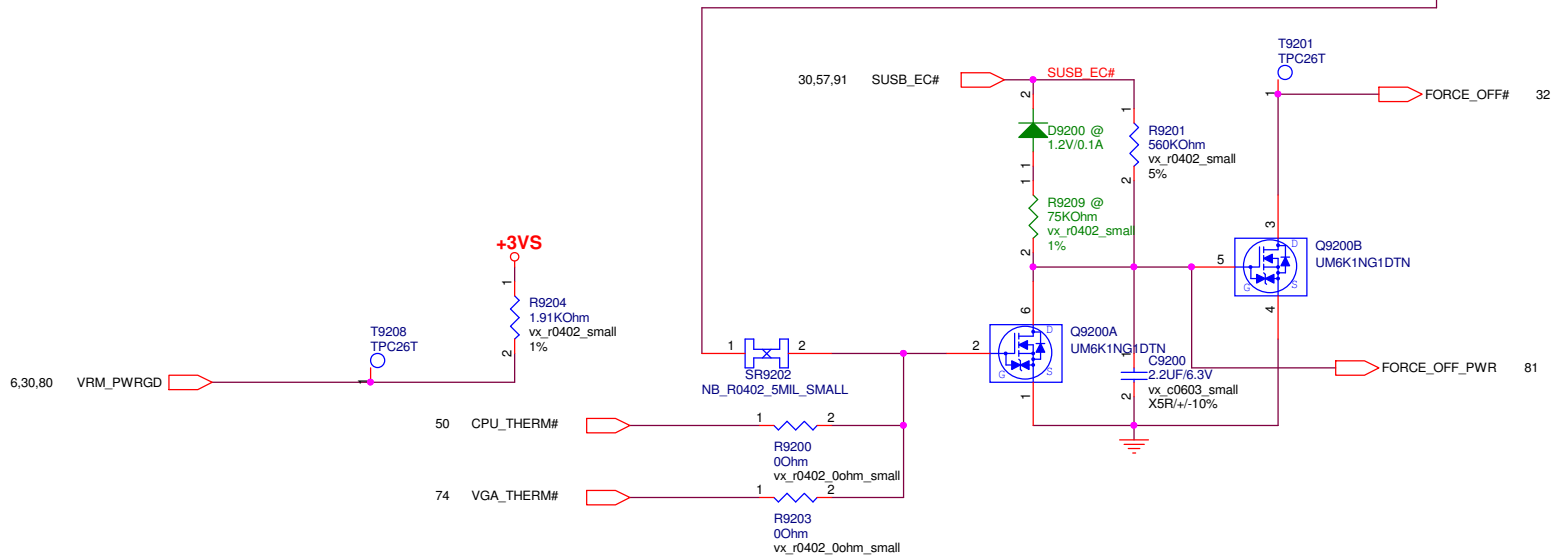
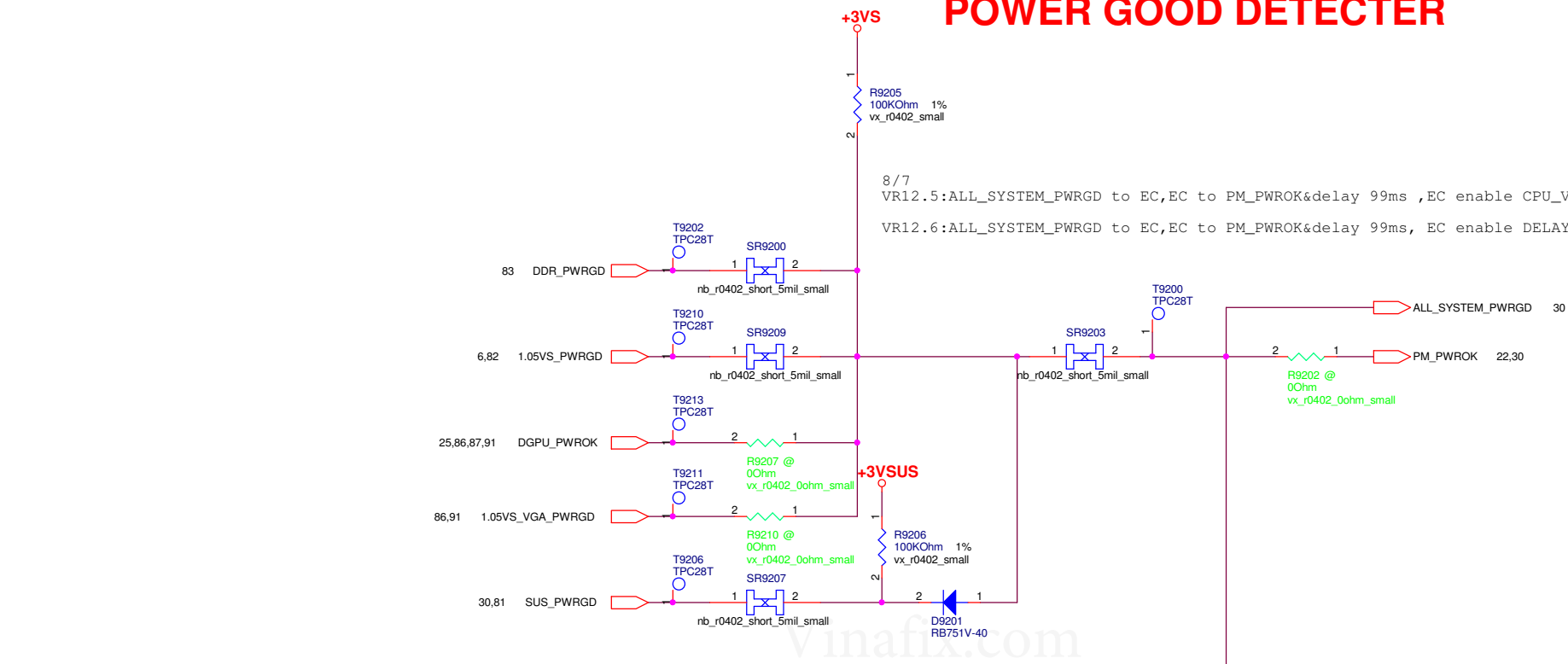
### DSC\_VGA\_PWR POWER Control

### SUSC#\_PWR POWER Control

<Variant Name>

PEGATRON PROPRIETARY AND CONFIDENTIAL			
Title : POWER_LOAD_SWITCH		Engineer: Neil Lin	
Size	Project Name	Rev	1.0
Custom			
Date: Friday, November 28, 2014		Sheet 91 of 96	

# POWER GOOD DETECTOR



<Variant Name>

<b>PEGATRON</b>		Title : <b>POWER_PROTECT</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		Engineer: <b>Neil Lin</b>	
Size <b>Custom</b>	Project Name <b>TRCUG</b>		Rev <b>1.0</b>
Date:	<b>Friday, November 28, 2014</b>	Sheet	<b>92 of 103</b>

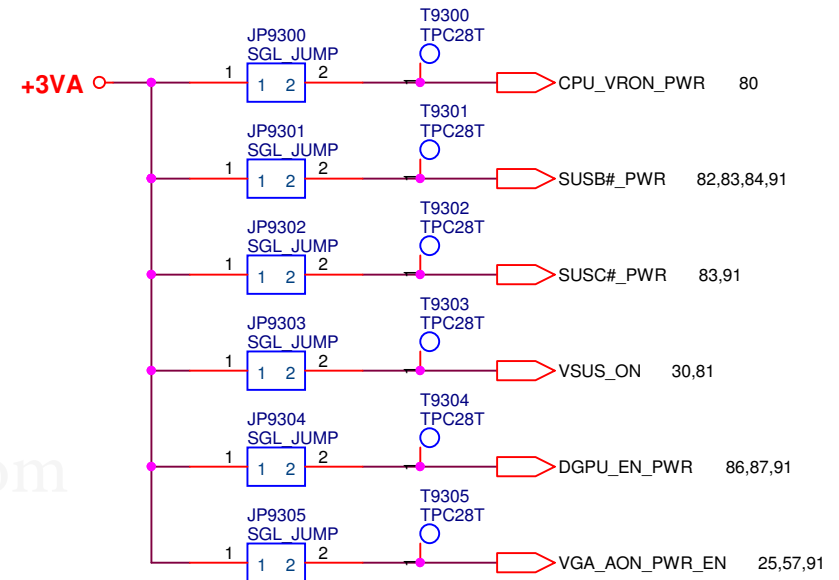
+A/D\_DOCK\_IN → +A/D\_DOCK\_IN 60,66,88  
+AC\_BAT\_SYS → +AC\_BAT\_SYS 20,45,80,81,83,87,88  
+BAT\_CON → +BAT\_CON 60,88  
+BAT → +BAT 88  
+5VA → +5VA 56,66,81  
+3VA → +3VA 20,26,30,32,56,57,60,66,81,88  
+5VO → +5VO 81,83,91  
+3VO → +3VO 81,82,84,86,91

+1.5VO → +1.5VO 84  
+1.35VO → +1.35VO 83,91  
+1.05VO → +1.05VO 82  
+0.675VO → +0.675VO 83  
+12VSUS → +12VSUS 26,81,91  
+5VSUS → +5VSUS 4,26,52,66,81  
+3VSUS → +3VSUS 22,26,28,30,36,53,81,92  
+3VS\_VGA → +3VS\_VGA 57,74,75,86,87,91  
+1.35VS\_VGA → +1.35VS\_VGA 57,71,75,76,77,91  
+3V → +3V 22,25,31,44,64,66,91

+1.35V → +1.35V 4,6,16,18,83  
+12VS → +12VS 25,28,31,48,91  
+5VS → +5VS 30,31,36,48,50,51,56,57,61,80,87,91  
+3VS → +3VS 6,16,17,20,21,22,23,25,26,28,30,31,36,37,40,45,48,50,53,57,61,62,64,66,80,91,92  
+1.5VS → +1.5VS 26,36,48,84  
+1.05VS → +1.05VS 6,25,26,80,82  
+0.675VS → +0.675VS 16,17,83  
+1.05VS\_VGA → +1.05VS\_VGA 57,70,71,72,86  
+1.05VO\_VGA → +1.05VO\_VGA 86  
+VGA\_VCORE → +VGA\_VCORE 57,75,87

+VCORE → +VCORE 6,80

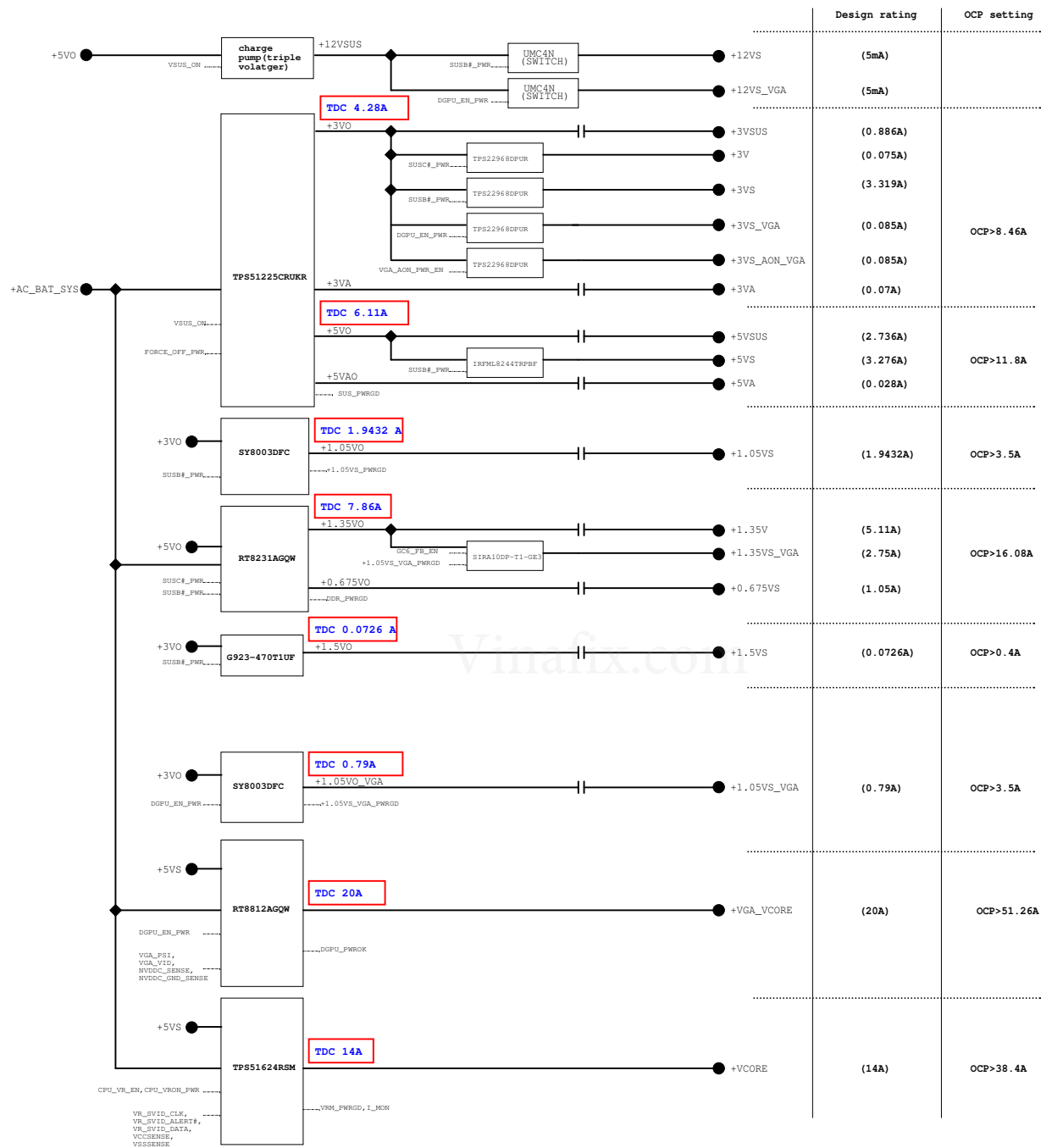
## FOR POWER TEST



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<Variant Name>

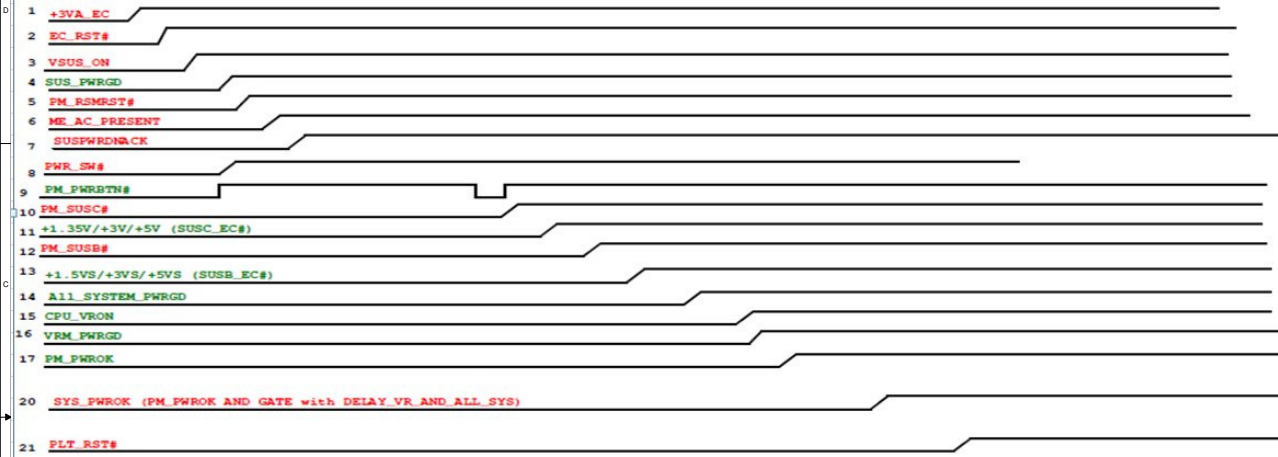
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PEGATRON PROPRIETARY AND CONFIDENTIAL			
Engineer: <b>Neil Lin</b>			
Size Custom	Project Name <b>TRCUG</b>		Rev 1.0
Date: <b>Friday, November 28, 2014</b>	Sheet <b>93</b> of <b>103</b>		



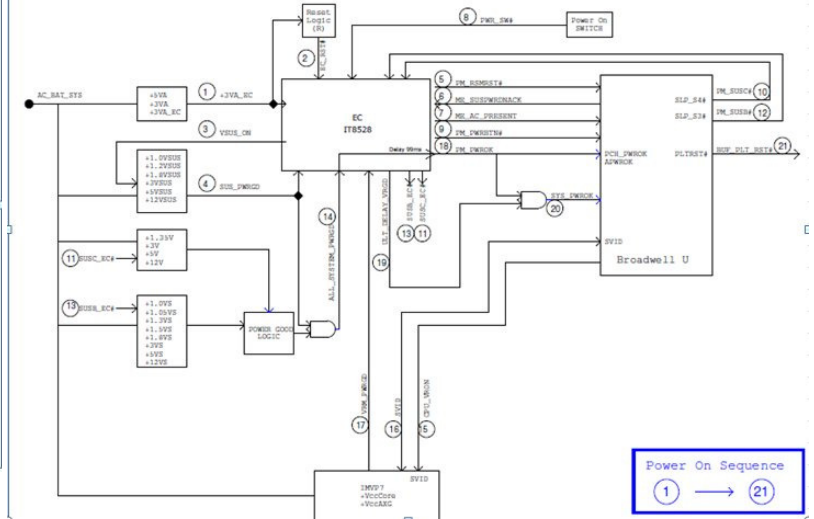
Modify notice		
Version	Date	Description
R1.1	2014/11/13	Change the size of Q870, Q874 and Q882 to 0027" from 0407"
R1.1	2014/11/13	Change Q820, Q832, Q833, Q844 and Q885 to SP42000070
R1.1	2014/11/13	Change Q810 from 0.12k to 0.20k
R1.1	2014/11/13	Change Q817 from 0.12k to 0.20k
R1.1	2014/11/13	Set Q810 and Q810 to avoid signal floating
R1.1	2014/11/13	Add Q810, Q811, Q812 and Q813 for D26 function
R1.1	2014/11/13	Q810 and Q811 are supported by T920204
R1.1	2014/11/13	Change Q817 from 0.12k to 0.20k
R1.1	2014/11/13	Set 4 off-page of VDD2_00_20 connecting to other page
R1.1	2014/11/13	Change Q820 from 470 00k to 100 00k
R1.1	2014/11/13	Change Q810 from 0 00k to 100 00k
R1.1	2014/11/13	Change Q811 from 0 00k to 100 00k
R1.1	2014/11/13	Change Q812 from 0.12k to 0.20k

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# G3 to S0- Power on Sequencing (Non -Deep Sx) AC-Mode



## Power On Sequence Diagram G3-S0 R0.1 [Non-iAMT, Non-Deep Sx]



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<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer:</b>	
Size	Project Name		Rev.
	Friday, November 28, 2014	97	102
Date	Sheet	of	

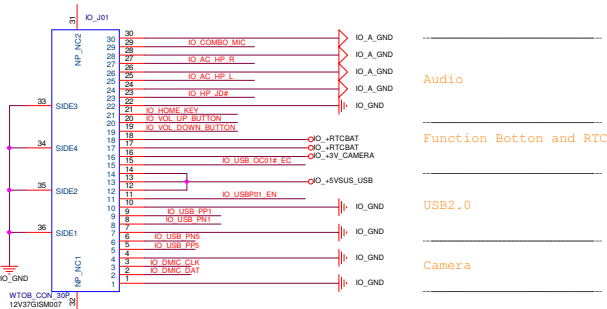
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<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer:</b>	
Size	Project Name		Rev.
	Friday, November 28, 2014	98	102
Date	Sheet		of

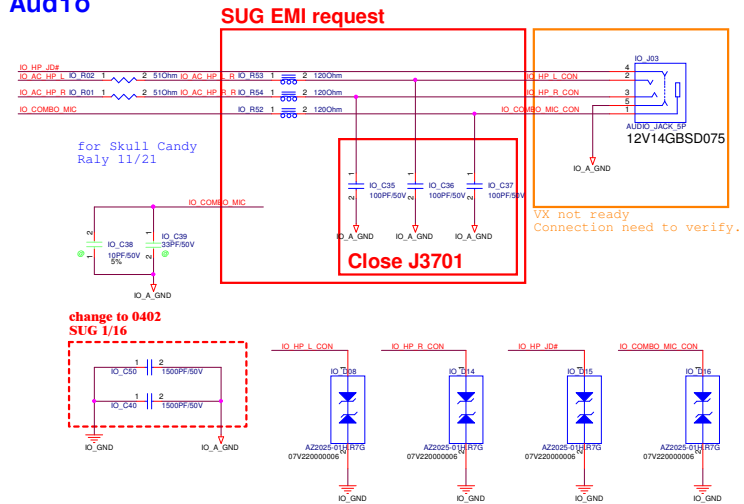
Vinafix.com

<Variant Name>			
<b>PEGATRON</b>		<b>Title :</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
		<b>Engineer:</b>	
Size	Project Name		Rev1.1
Date		Friday, November 28, 2014	
Sheet		99	of 102

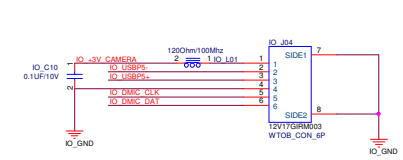
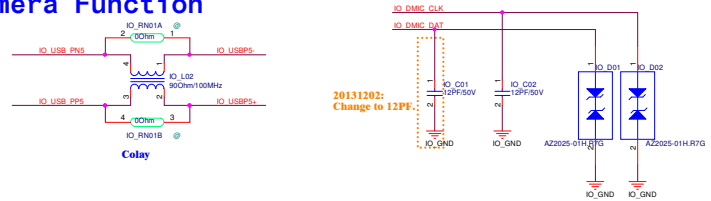
## Connector



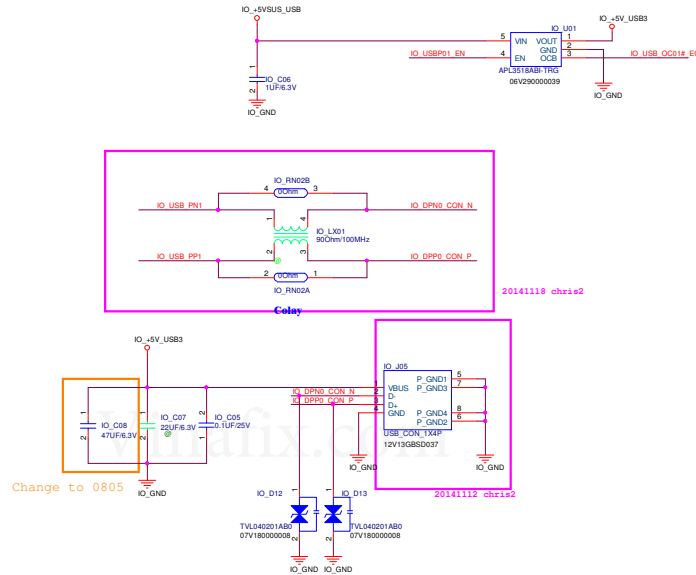
## Audio



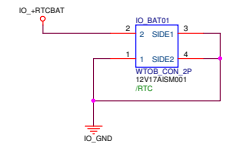
## Camera Function



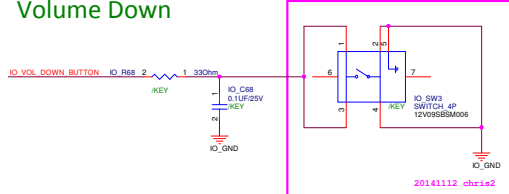
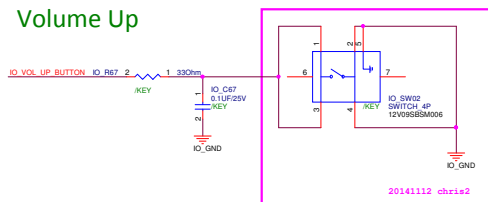
## USB2.0 Port



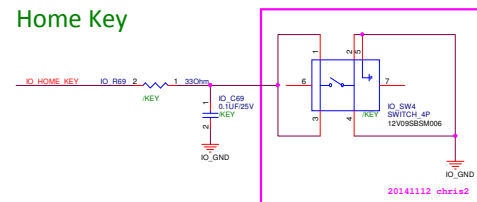
## RTC Wire Connector



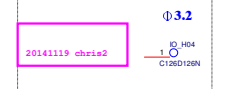
## Convertible Key



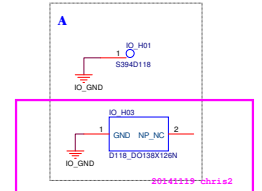
## Home Key



## PCB Tooling HOLE



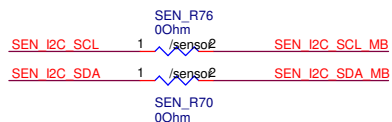
## PCB SCREW HOLE



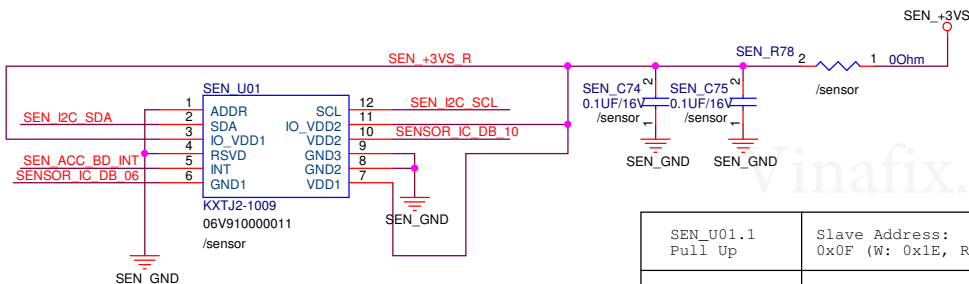


## I2C Repeater

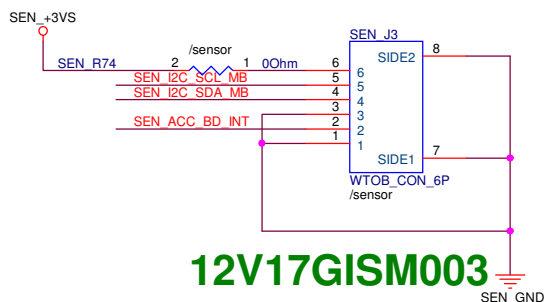
20141227 Chris2



## G-Sensor

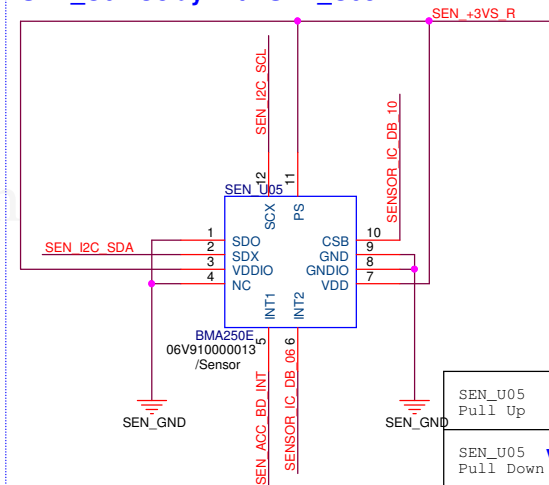


SEN_U01.1 Pull Up	Slave Address: 0x0F (W: 0x1E, R: 0x1F)
SEN_U01.1 Pull Down	Slave Address: 0x0E (W: 0x1C, R: 0x1D)

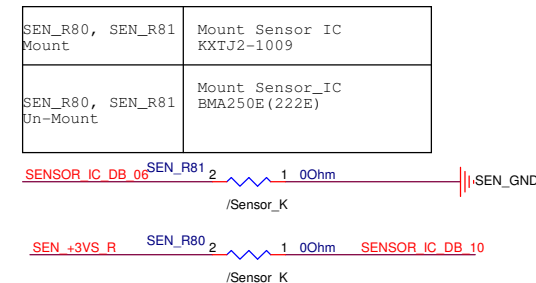


12V17GISM003

## SEN\_U01 Colay with SEN\_U05



SEN_U05 Pull Up	Slave Address: 0x19 (W: 0x32, R: 0x33)
SEN_U05 Pull Down	Slave Address: 0x18 (W: 0x30, R: 0x31)



SEN_R80, SEN_R81 Mount	Mount Sensor IC KXTJ2-1009
SEN_R80, SEN_R81 Un-Mount	Mount Sensor_IC BMA250E (222E)

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<Variant Name>

<b>PEGATRON</b>		Title : <b>G-Sensor BD</b>	
PEGATRON PROPRIETARY AND CONFIDENTIAL			
<OrgName>		Engineer: <b>Mike Pan</b>	
Size <b>B</b>	Project Name <b>ES10AC/ACL</b>		Rev <b>0.5</b>
Date: <b>Friday, November 28, 2014</b>		Sheet <b>103</b> of <b>103</b>	